



397 Route 281 – P.O. Box 1175

Tully, New York 13159-1175

Phone: 315 696-6676

Fax: 315 696 9923

Email: sales@acipower.com

www.acipower.com

APPLICATION NOTE

AC2/AC5/AC7/ACN SERIES CCFL INVERTERS

3/2/09

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- INTRODUCTION:

The following application note is intended primarily for the user of an AC2, AC5, AC7 or ACN series inverter. Most of the information contained within however, is applicable for many of our custom products as well. Please consult the **Data Sheet** specifically for your inverter for any additional information.

On the surface, the function of the inverter and its interconnection with the tubes and application may seem trivial, do not be fooled! Conceptually these products are straightforward. It has been our experience however, that underestimating a component able to convert what can be 35 watts of power, produce voltages in excess of 2500Vrms, and that in many cases interfaces with the video world can fray many a nerve. If you don't read anything else, please take notice always of the following points:

1. Know where the high voltage is and understand the need for spacing and/or insulation in critical areas.
2. Know the inverter(s) input current requirements. A 12V unit can require over 3 amps (X2 if a Master/Slave configuration is used). This is not a trivial amount of current and it can be pulsing 100 times a second if dimming is employed. A vast majority of problems fall into this category due to poor grounding practices and interaction with sensitive circuitry in the user application. **Separate power and return paths from the power source to the inverter(s) cannot be overstressed.**
3. Think cool. In backlighting a flatpanel application, many times minimalist profiles create cooling concessions. Not only is it important on the inverter side for reliability, more often excessive heat at the CCFL's can cause them to decrease in light output resulting in an overall inefficient backlight system.
4. We are very flexible. Most of our products are micro-controller based which among other things allows us to take in consideration control issues the user may have not planned for or does not want to support.
5. CCFL current levels adjusted easily. Both AC2 and AC5 can be tailored to meet your brightness requirements in a turnkey fashion. Both series have clearly defined performance specifications. When custom packaging and/or functionality is required, we can quickly help to define the product and provide it in a timely fashion.

GENERAL PRODUCT INFORMATION:

All AC2, AC5 & ACN inverters are constructed on a 0.062 inch FR4(94V-0) PCB material (0.050 inch for AC7). They have 0.120 inch mounting holes. Only on AC5 are two of the four mounting holes tied to input ground. As of the writing of this application note, **AC5 is a UL 1950 recognized component (File No. E201813)**. AC2 is pending recognition.

AC5 in its standard configuration has right-angle Molex 0.100-inch connectors for input and output. The board can be specified with a wide variety of interconnection schemes including straight up, pcb mountable and flying lead. When required, many other connectors will fit if they conform to 0.100-inch spacing.

AC2 in its standard configuration is the same as AC5 except the input connector is a surface-mount, 0.05 inch pitch right-angle header. The only other input connector option for the AC2 and ACN is a straight-up version of the same style. Both AC2 & AC5 are less than 0.575 inches in total profile. Options for heat sinking of the power-mosfets on AC5 as well as off-the-board ballast capacitors can be accommodated.

AC7 in its standard configuration has a right-angle Molex 0.100-inch connector for its input and 1 or 2 JST output connectors. AC7's nominal profile is 0.350 inches.

ACN in its standard configuration has a right-angle Molex surface-mount, 0.05 inch pitch right-angle header the same as AC2. On the opposite end of the PCB is 1 JST output connector that will service 1 or 2 CCFL's. ACN's nominal profile is 0.552 inches

STANDARD INPUT CONNECTOR (CON 1) PIN ASSIGNMENTS:

The standard Connector 1 pin assignments are as follows:

AC2/ACN

<u>Pin</u>	<u>Function</u>
1	+Vin
2	+Vin
3	Gnd
4	Gnd
5	Enable
6	Vcntl
7	Logic Hi / +5Vout
8	Pwm Out

AC5

<u>Pin</u>	<u>Function</u>
1	+Vin
2	Gnd
3	Enable
4	Logic Hi / +5Vout
5	Vcntl
6	Pwm Out

AC7

<u>Pin</u>	<u>Function</u>
1	+Vin
2	Gnd
3	Vcntl
4	Logic Hi / +5Vout

PIN DEFINITIONS:

+VIN,GND

These are the positive power and ground input pins. On AC2 & ACN, maximum current per pin is 1.0 amp. On AC5 & AC7, the maximum current per pin is 4.0 amps. In the case of the AC5, be aware that the mating connector/terminal you select will determine the maximum current per interconnection. In general, standard brass terminals are rated at 2.5 amps whereas phosphor bronze terminals are rated typically at 4.0 amps. Because of the variety within the Molex family as well as compatible substitutes; i.e. Amp, Berg, Methode, etc., please consult the appropriate data sheets. ACI will be happy to assist you in this endeavor.

ENABLE

This is a CMOS/TTL compatible input. It is active high and has no on-board pull-up. This pin must be high for the inverter to operate. If not implemented **it should not be left floating**, rather tie it to an external +5V source or the Logic Hi pin (Pin 7 on AC2/ACN, Pin 4 on AC5/AC7). Also note this pin functions as the PWM input pin when configured in “Slave Mode” for AC2, AC5 & CAN series inverters. Refer to figure 1 in the connection diagram section of this application note.

LOGIC HI / +5VOUT

This is a CMOS output provided as a convenience to the user who may need +5V for use with the intensity potentiometer or for low current logic level purposes. Maximum current draw should be limited to 1mA. If more current is desired, up to 50mA can be drawn if an on-board jumper is installed. For AC2, the jumper designation is JP3, for AC5 it is JP4. ACN & AC7 must be configured at the factory if the full 50mA capability is required.

VCNTL

This pin is where the 0 to +5V intensity control signal is applied. 0V input corresponds to a 0% duty cycle(CCFL's off) and +5V is 100%(CCFL's full on) There are 255 discrete and equally weighted duty-cycle steps as the control voltage is varied from 0 to +5V. A firmware algorithm ensures that a voltage presented to the Vcntl input that is midway between quantization levels will not create instability/dithering of the pwm-dimming signal and hence erratic “flicker” of the CCFL's. Care should be taken however, that noise is kept to a minimum on this input so as not to “overload” the firmware algorithm. A potential side effect would show up as non-responsiveness to intensity control changes.

If the source of Vcntl is external to the inverter board as would be the case with a D/A or Digital pot residing on the users pcb, during system power-up, a control voltage might be presented to the Vcntl input in advance of the inverter powering up. This situation can lead to the users application “backfeeding” the on-board micro-controller and preventing it from doing a proper power-up/reset. It is therefore recommended in these situations that a 10k resistor be placed in series with the Vcntl line. Refer to figure 2 in the connection diagrams section of this application note. When using an external potentiometer, a value of 10k is recommended. Normally it should be connected as follows:

1. High side of pot to Logic Hi / +5V Out
2. Wiper to Vcntl
3. Low side of pot to Gnd at inverter

In the event of long lead lengths (18 inches or more) or high noise environments, some additional bypassing may be required. Contact the factory if there is a concern in this area that may require a larger value of decoupling capacitance than the standard on-board 0.1uF.

PWM OUT

This is a CMOS output signal provided mainly for use when two inverters are employed in a Master/Slave configuration. Typically this signal is fed to the Enable pin of a second inverter configured as a Slave. As the voltage presented to the Vcntl pin is varied, a proportional duty-cycle change will be seen at this pin. Consult figure 1 in the Connection Diagrams section of this application note.

OPTIONAL CON 1 PIN FUNCTIONS:

VSYNC IN

On all inverters where specified, this function would be supported in place of the Logic High / +5V output pin. Typically the user would connect the vertical synchronization pulse provided by the LCD and/or LCD Controller. With this signal present, the inverters pwm frequency will lock and be that of the LCD. This may be desirable in cases where a vertically moving band appears due to the PWM frequency of the CCFL's strobing the displays frame rate. It is generally good practice to place a 10k resistor between this input and the source of the Vsync signal. This will greatly reduce unwanted current and noise from false triggering the inverter circuitry. Refer to figure 2 in the connection diagrams section of this application note. If this pin is implemented but not used, it should be tied to +5V. Normally the standard asynchronous frequency of the inverters (98Hz) has been chosen such that this interference should not occur. It should be noted that the user will lose the ability to obtain a source of Logic High / +5V. If it is required and the application does not require two inverters in a Master/Slave configuration, the PWM Out pin can be programmed hi for use as Logic High (Please contact factory for this option). Alternatively, if two units are used in a Master/Slave arrangement, Logic Hi / +5V can be obtained from the slave unit. (Note: When implementing Vsync on AC7 inverters, the user will have to provide his own source of +5V if needed.)

On AC2 and ACN, pins 5 thru 8 and on AC5 pins 3 thru 6 although configured as described above, can be different if the users application demands it. A few examples of functions that may be desirable and can be easily supported are: Serial communication, simple hi/lo to 4bit (16 step) intensity control, light/temperature sensor interfaces, heater control, push-button control. AC7 also has the same flexibility but is limited to alternate uses of pins 3 and 4 only.

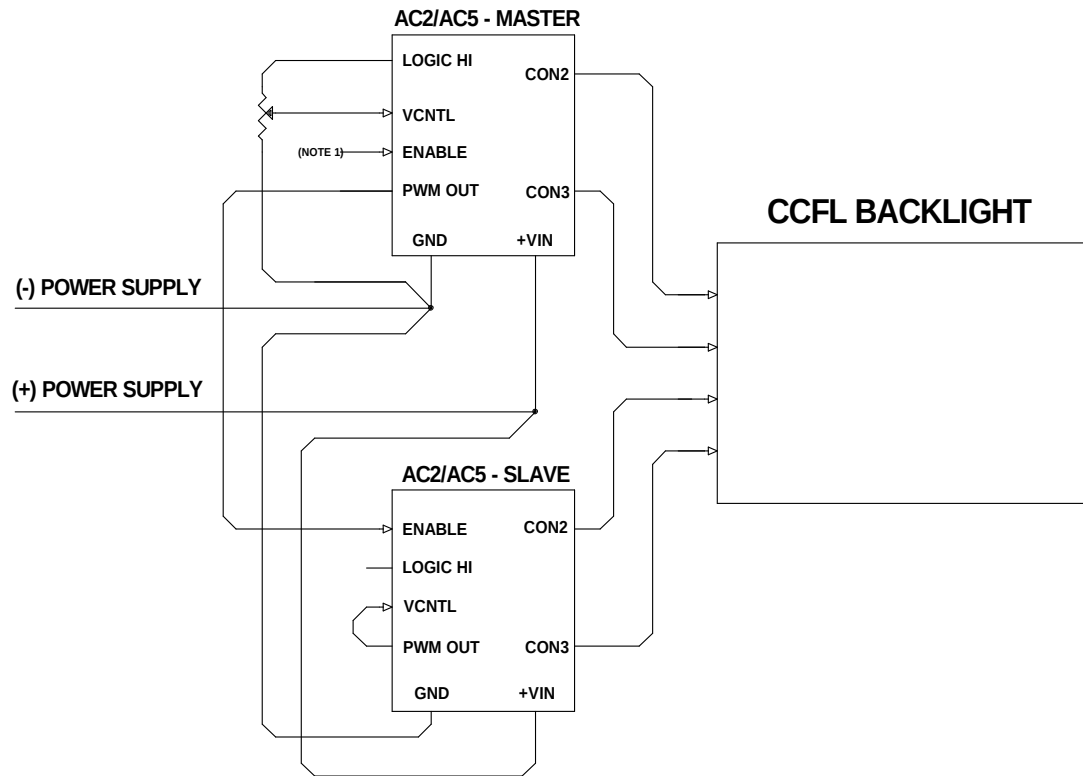
MASTER/SLAVE OPERATION:

AC2, AC5 and ACN can be used in a Master/Slave mode. This mode allows the use of multiple inverters operating as one integrated system. This would be necessary when the applications CCFL power requirements or number of tubes exceed that of what one inverter could supply. The benefit of Master/Slave mode is synchronization of the dimming control signals. Typically one inverter is designated as the “Master” by virtue of the connections made to it via CON1. All of the users control signals would route to the Master (I.E. Enable, Vcntl, Vsync if employed, etc.). The 2nd inverter would be designated as the “Slave” again by virtue of its connections via CON1. Typically the Slave unit(s) require only power & ground plus a pwm signal generated by the Master. An additional connection is made at the Slaves input connector from its Vcntl input to its Pwm output. Upon power-up this connection will allow the unit to go into “Slave mode” and thus configure the Enable input to accept the Pwm signal from the Master. NOTE: WHEN USING AC5 SERIES INVERTERS REVISION D OR HIGHER, THE MASTER/SLAVE JUMPER MUST ALSO BE INSTALLED.

AC7 series inverters also have the ability to be used in Master/Slave mode. Since I/O is limited to only two pins, please consult the factory so we may provide you the best flexibility for your application.

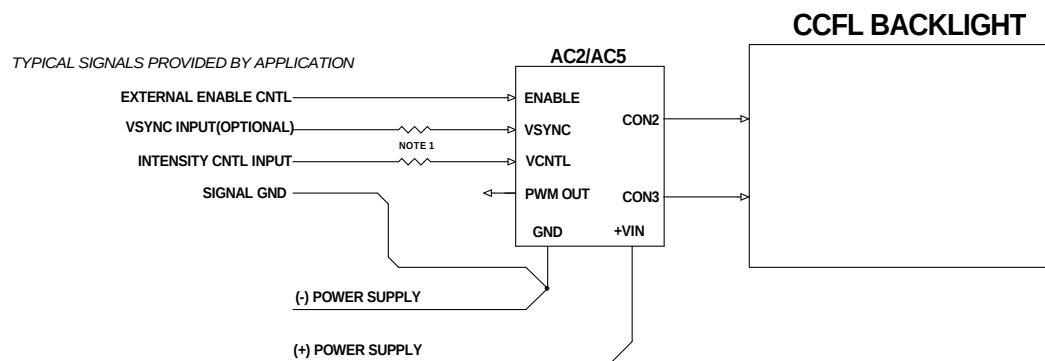
CONNECTION DIAGRAMS:

Figure 1 – AC2/AC5/ACN in Master/Slave Mode



NOTE 1: IF ENABLE CONTROL NOT USED, TIE TO LOGIC HI. DO NOT ALLOW TO FLOAT

Figure 2 – AC2/AC5/ACN standard input control signals



NOTE 1: RECOMMENDED 10K NOMINAL REQUIRED FOR NOISE IMMUNITY

DO'S & DON'TS

1. Do not run leads from CON1 near the output connectors or around the transformer(s). Pay particular attention in not allowing these leads to run under the PC board where they may come in contact with high voltage traces.
2. When mounting inverter, do not allow bottom of PCB to come closer than **5mm (0.197 Inches)** to any conductive surface unless a suitable insulator is used.
3. Do not modify or change any of the high voltage ballast capacitors. They are conformal coated and should not be contaminated in any way.
4. Do not allow the transformer(s) to come in contact with any metallic surfaces nor should any attempt be made to heat sink them unless a suitable insulating material is used. Please contact the factory if you feel your application requires this.
5. Do keep lead lengths as short as possible.
6. Do not mix power grounds with signal grounds.
7. Do not allow control signal inputs to exceed 6.5V.

FLICKER

Numerous definitions of flicker exist within the flatpanel display community. Contemporary usage has come to describe just about any abnormality of the image on the LCD as it interacts with the CCFL backlight. Anything having an erratic or repetitive quality that detracts from the viewed image has been dubbed flicker. The following list comprises many of the root causes that get diagnosed as “flicker”:

1. Electrical coupling or noise pickup of the LCD supply voltage(s) due to the relatively high currents demanded by the Inverter (i.e. Poor/No separate power and return path to the Inverter module).
2. Strobing or Beat Frequency of CCFL chopping frequency with the LCD vertical/refresh rate.
3. Insufficient starting voltage available **at** the CCFL's. Long CCFL leads and/or parasitic capacitance of these leads can rob the CCFL's of the starting voltage that is developed at the inverter.
4. Capacitive coupling of the CCFL's to other CCFL's and their enclosure. Highly dependent upon the design and construction of the backlight system.
5. Non-stable PWM dimming control signal (when user supplied).
6. Poor regulation/dynamic response of user power supply.
7. Floating or noise pick-up on the enable line or if so equipped, the Vsync input line.
8. Arcing anywhere in the high voltage path including wires, connectors or insufficient PCB clearances.

Many times more than one of these items will present themselves in the user application and make troubleshooting difficult at best. ACI experience to date determined the order of the above list with the most likely causes starting at the top. Because every backlighting application is unique, we highly encourage you to contact us so we can help solve flicker issues should they arise.

For those of you that like a good challenge, determine first if the problem exists when the LCD is not active. This would rule out items 1 & 2 above. Then verify that you have a stable supply voltage and the control lines to the inverter are being operated correctly (Items 6 & 7). Minor changes to the input voltage of the inverter will affect starting voltage and help to pinpoint problems related to Items 3 and 4.

While the above guide is by no means all encompassing, a vast majority of flicker issues fall within the categories listed. ACI is also happy to assist in the characterization/troubleshooting of your application if it can be made available to us.