



Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	14.1" WXGA+ Color TFT-LCD
Model Name	B141PW04 V0
Note ()	<i>LED Backlight with driving circuit design</i>

Customer	Date
Checked & Approved by	Date
Note: This Specification is subject to change without notice.	

Approved by	Date
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Product Specification

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/09/01	All	First Edition for Customer		

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B141PW04 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the WXGA+ (1440(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B141PW04 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	357.7 (14.1W")			
Active Area	[mm]	303.48 (H) x 189.68 (V)			
Pixels H x V		1440 x 3 (RGB) x 900			
Pixel Pitch	[mm]	0.2108 x 0.2108			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED=20mA) (Note: ILED is LED current)	[cd/m ²]	280 typ. (5 points average) 240 min. (5 points average)(Note1)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		350 min			
Response Time	[ms]	8 typ / 15 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	5.5 max. (Include Logic and Blu power, without LED efficiency))			
Weight	[Grams]	375 max.			
Physical Size	[mm]		L	W	T
		Max	320.0	207.0	5.5
		Typical	319.5	206.5	-
		Min	319.0	206.0	-
Electrical Interface		2 channel LVDS			
Surface Treatment		Anti-Glare, Hardness 3H, Haze 11%			
Support Color		262K colors (RGB 6-bit)			



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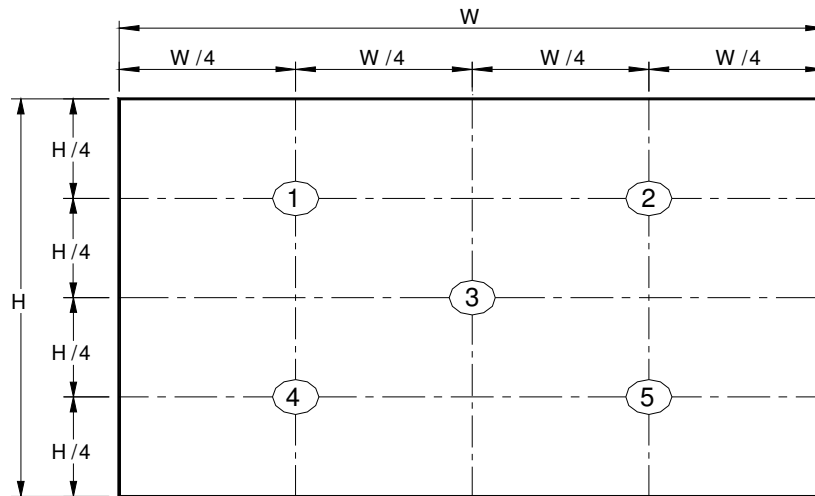
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

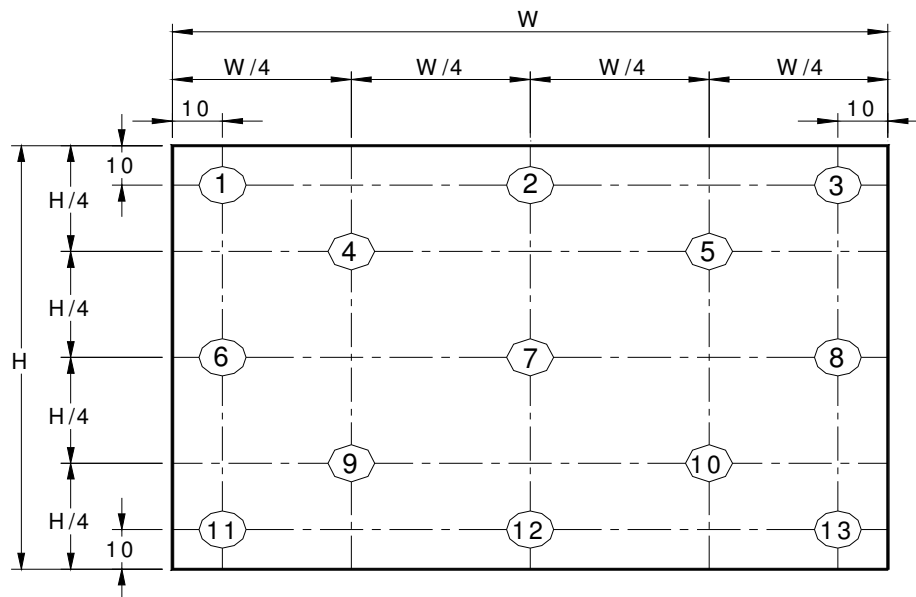
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance (ILED=20mA)	[cd/m ²]	5 points average	240	280	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right)	-	40	-	4, 9
	[degree]	CR = 10 (Left)	-	40	-	
	[degree]	Vertical (Upper)	-	15	-	
	[degree]	CR = 10 (Lower)	-	30	-	
Luminance Uniformity		5 Points	-	-	1.25	1, 3, 4
Luminance Uniformity		13 Points	-	-	1.53	2, 3, 4
CR: Contrast Ratio			350	-	-	4, 6
Cross talk	%				4	4, 7
Response Time	[msec]	Rising	-	-	-	4, 8
	[msec]	Falling	-	-	-	
	[msec]	Rising + Falling	-	8	15	
Chromaticity of color Coordinates (CIE 1931)		Red x	0.550	0.580	0.610	4, 9
		Red y	0.310	0.340	0.370	
		Green x	0.280	0.310	0.340	
		Green y	0.520	0.550	0.580	
		Blue x	0.125	0.155	0.185	
		Blue y	0.125	0.155	0.185	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

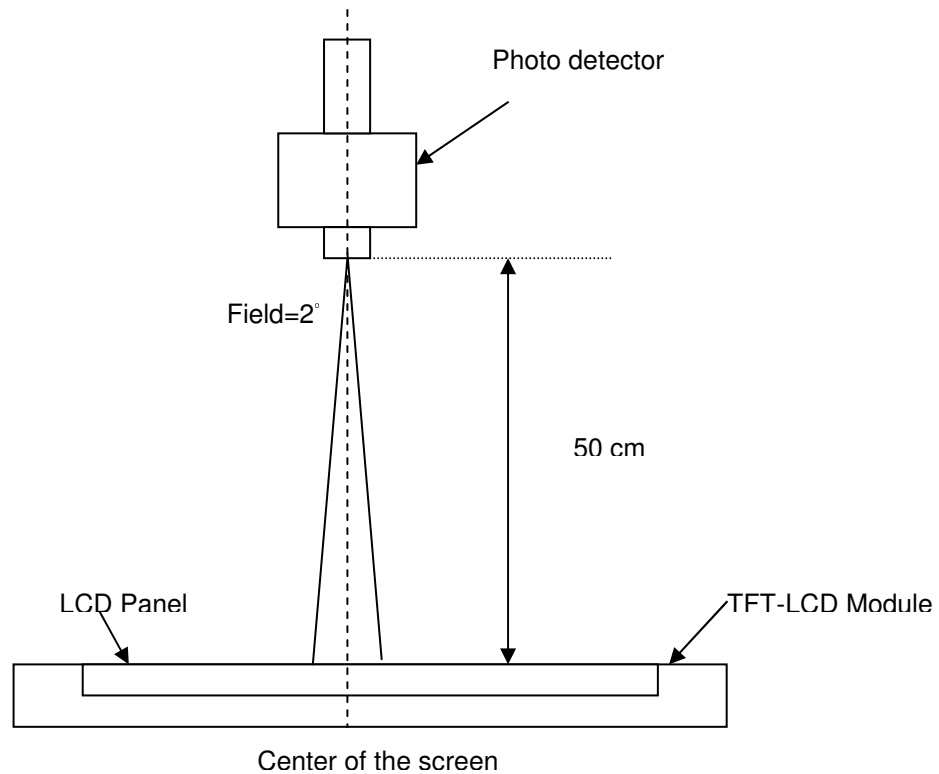
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

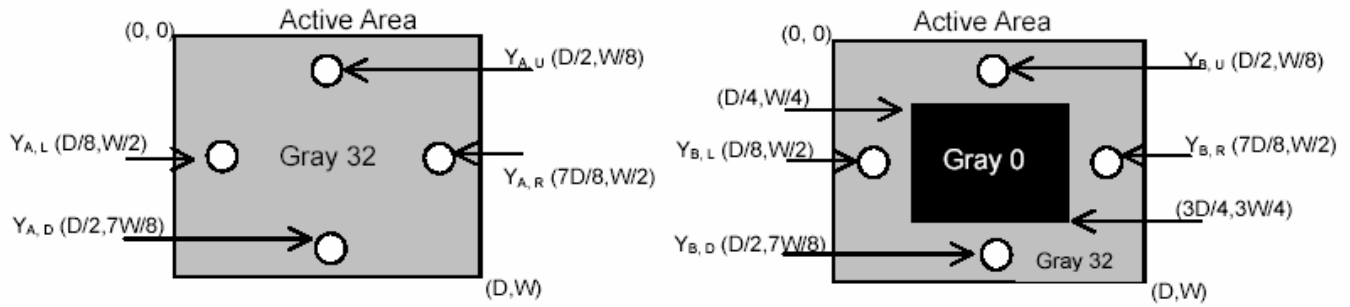
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

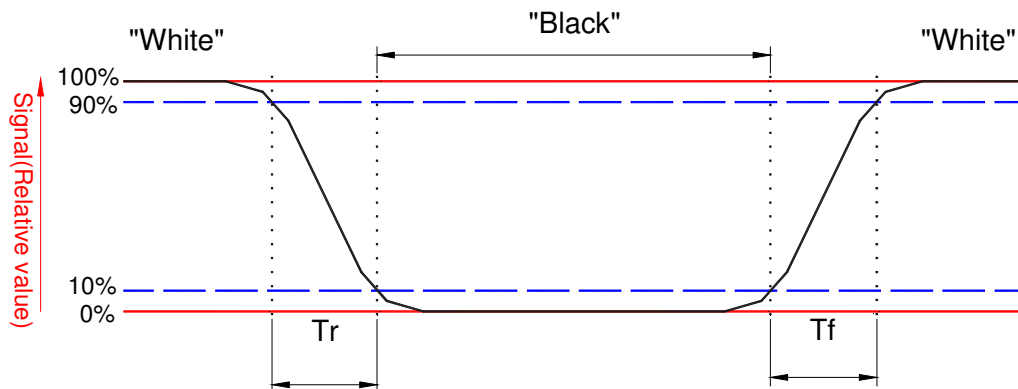
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



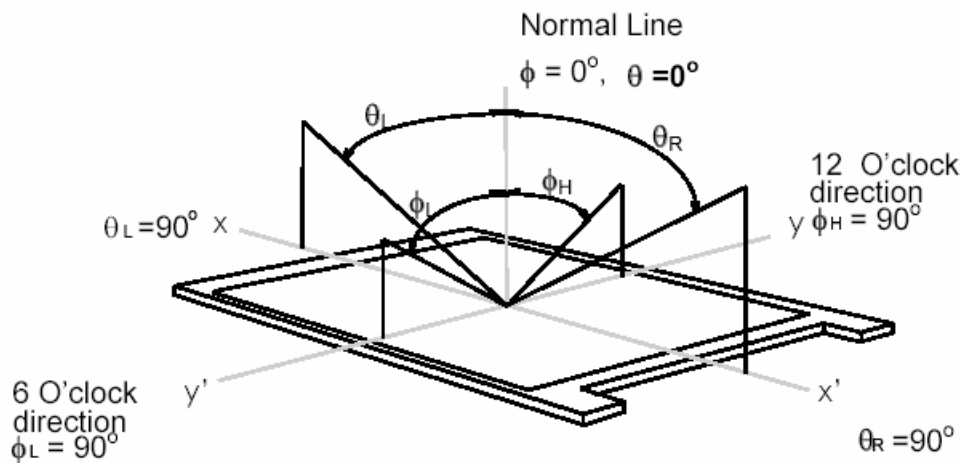
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



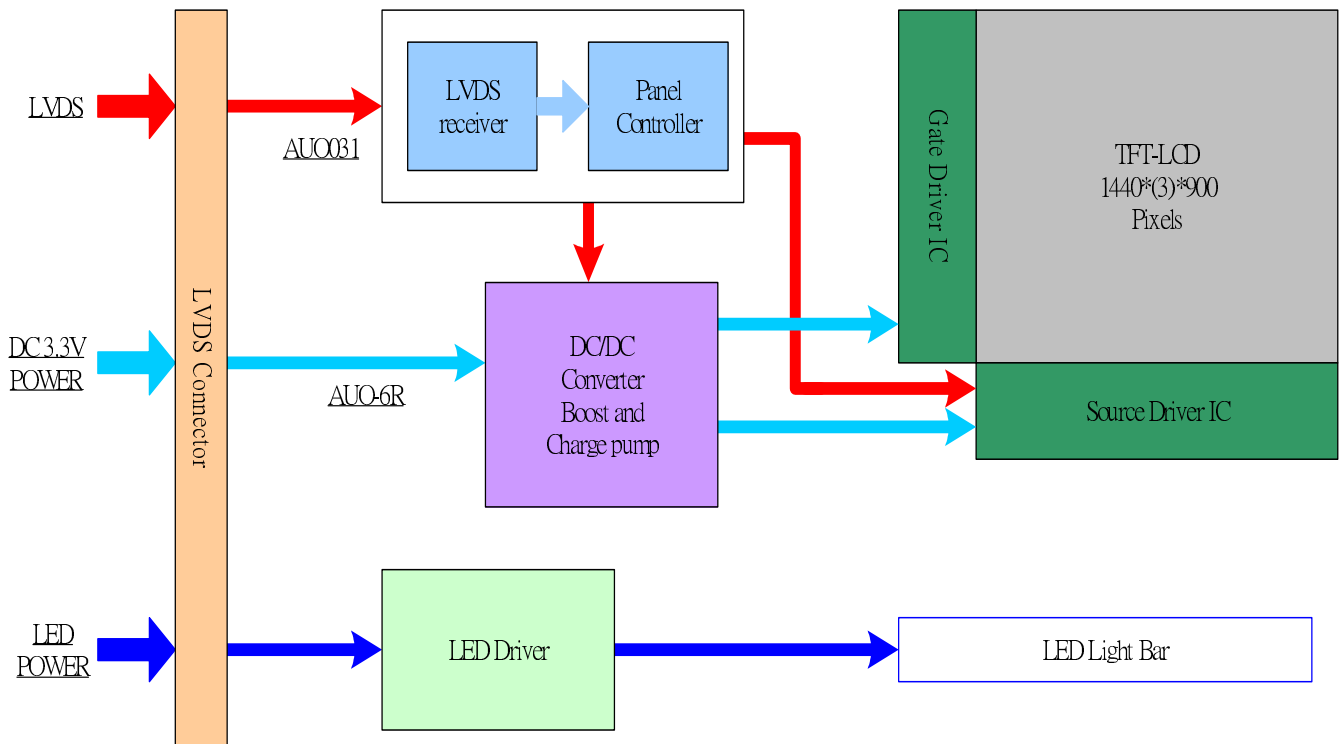
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

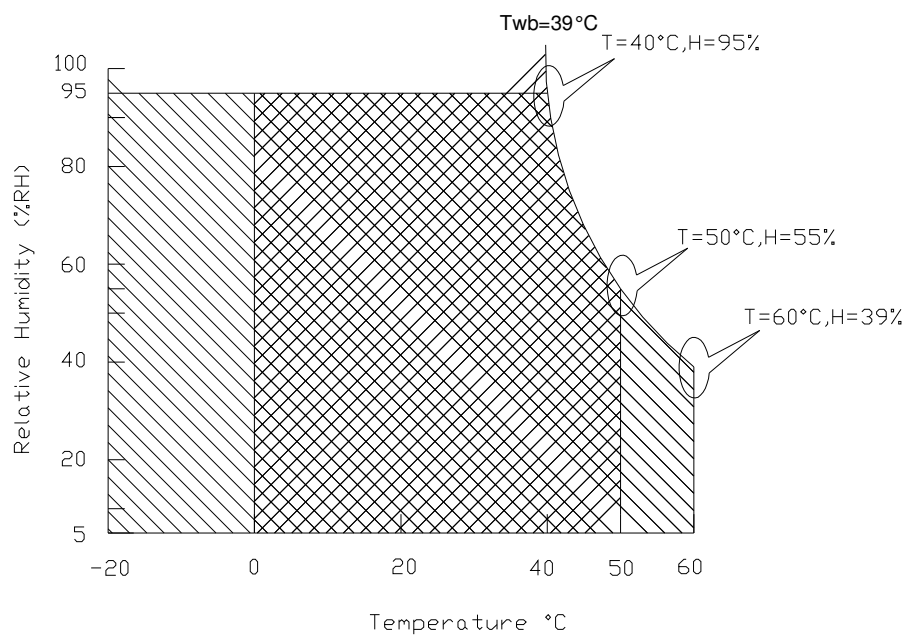
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

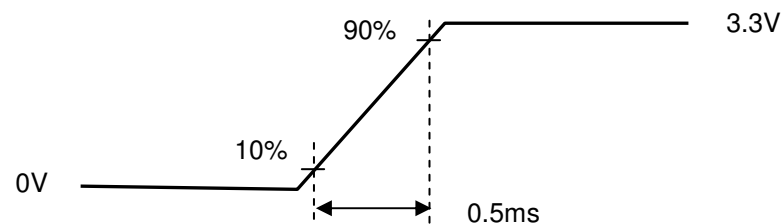
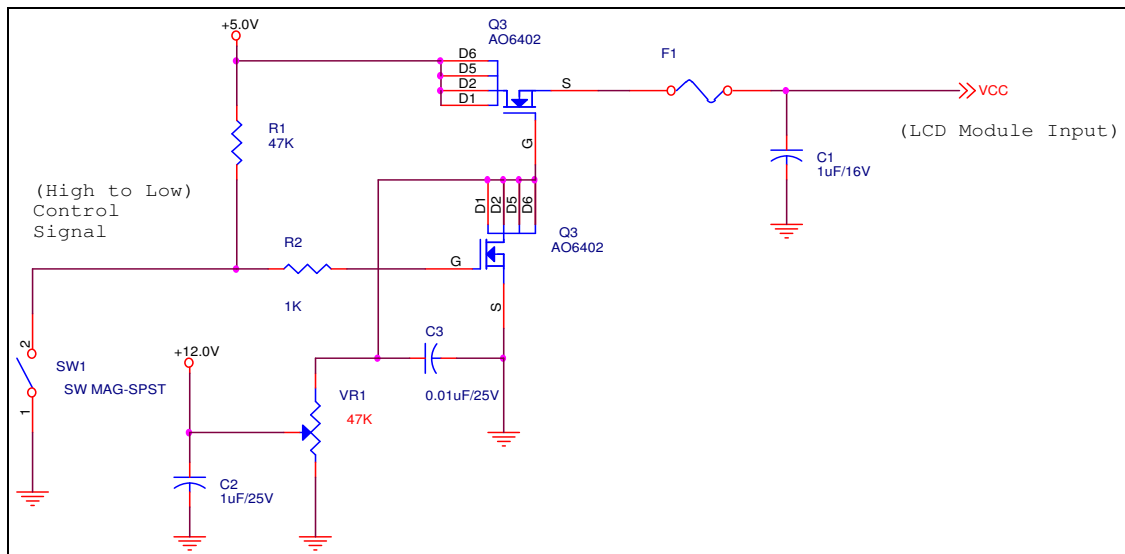
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.5	[Watt]	Note 1/2
IDD	IDD Current	-	310	415	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

5.1.2 Signal Electrical Characteristics

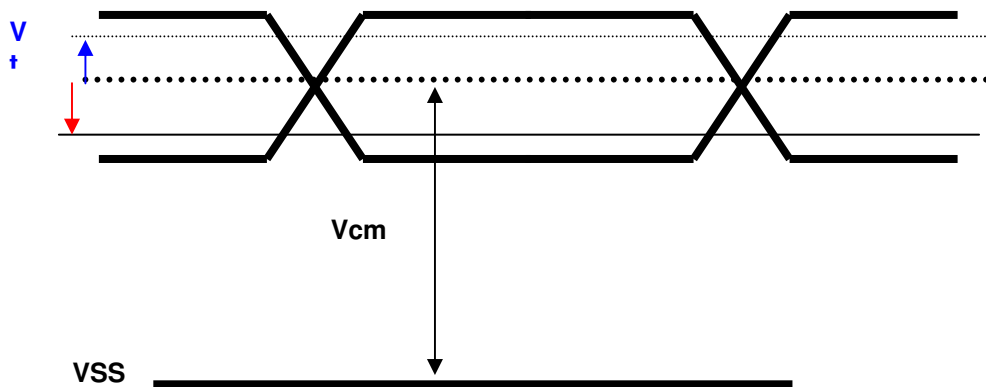
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold ($V_{cm}=+1.2V$)	-	100	[mV]
Vtl	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	1.1	1.45	[V]

Note: LVDS Signal Waveform





5.2 Backlight Unit

LED Parameter guideline for LED driving selection

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	2.8	3.2	3.5	[Volt]	(Ta=25°C)
LED Forward Current	I_F		20	20.6	[mA]	(Ta=25°C)
LED Power consumption	P_{LED}		3.456		[Watt]	(Ta=25°C) Note 1
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C) $I_F=20\text{ mA}$ Note 2

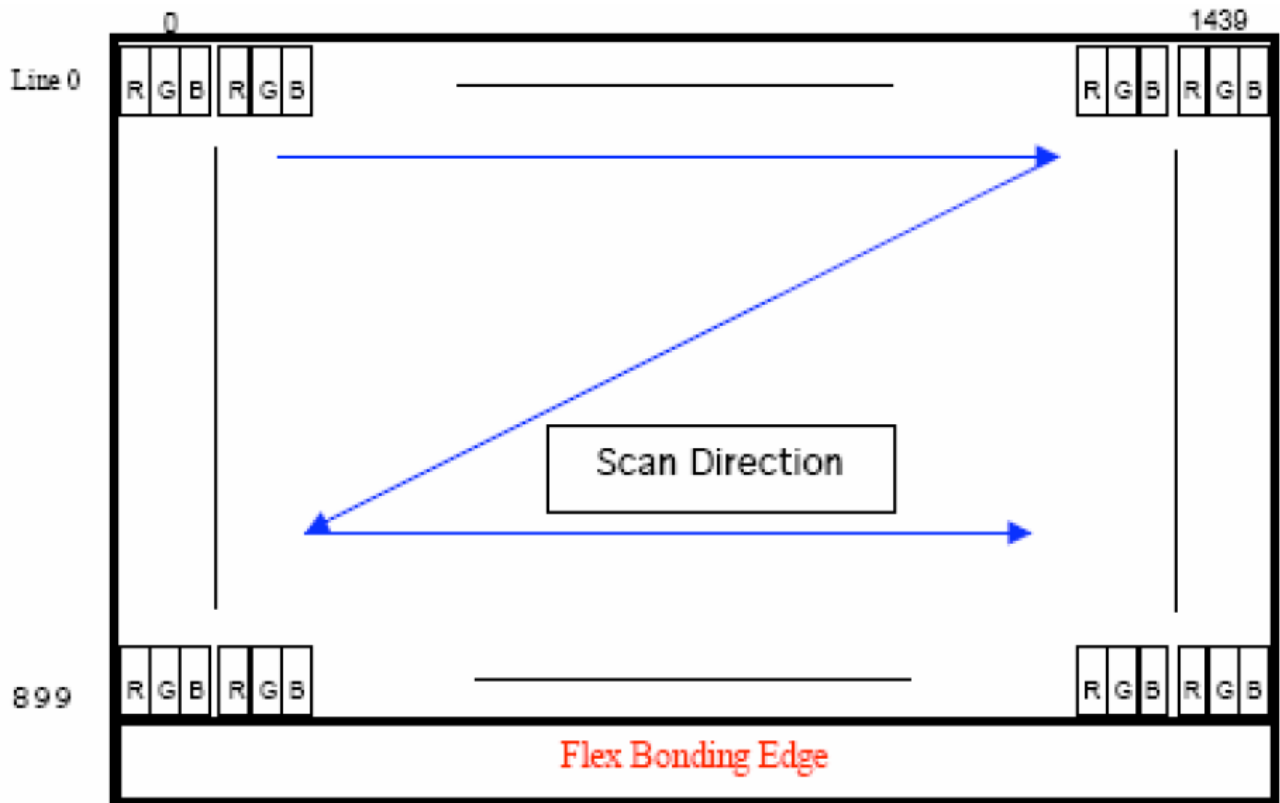
Note 1: Calculator value for reference $P_{LED} = I_F \times V_F \times LED(Qty)$

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

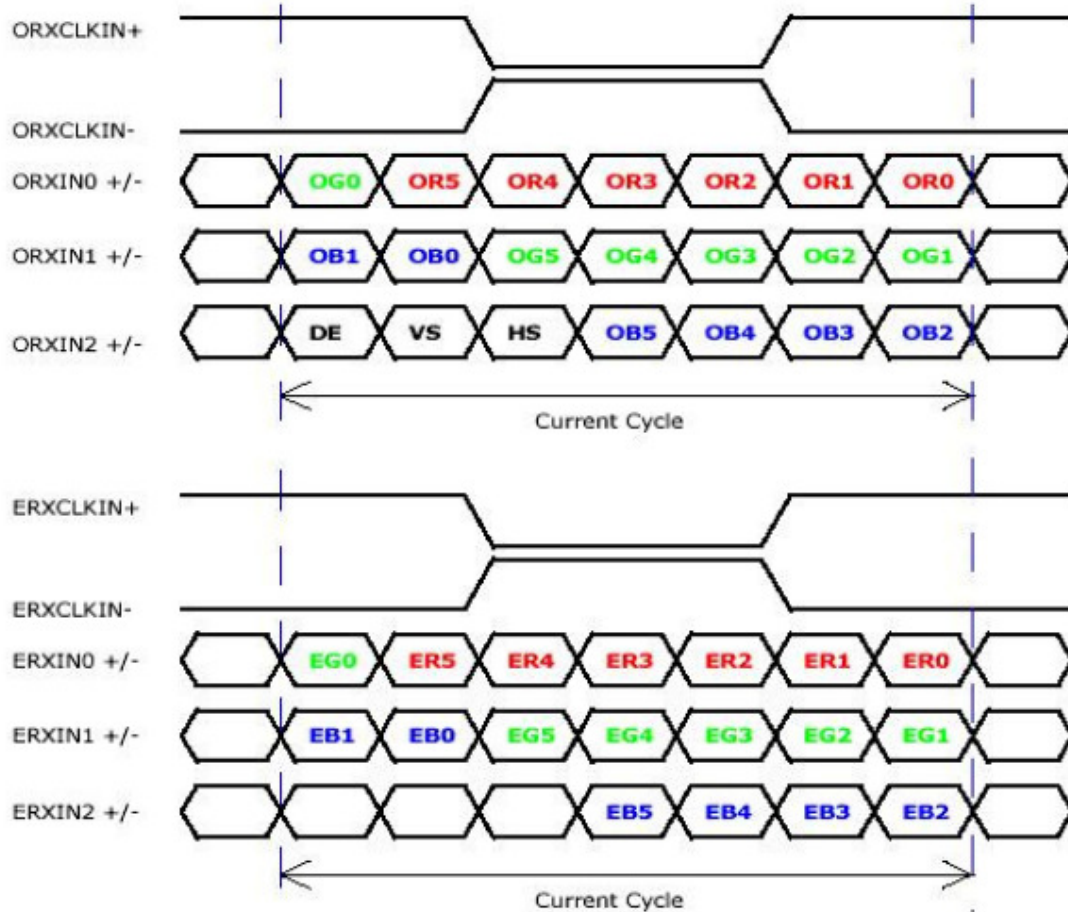
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description
V _{EDID}	+3.3V EDID Power
CLK _{EDID}	EDID Clock Input
DATA _{EDID}	EDID Data Input
ORXIN0-, ORXIN0+	Odd LVDS differential data input(ORed0-ORed5, OGreen0)
ORXIN1-, ORXIN1+	Odd LVDS differential data input(OGreen1-OGreen5, OBlue0-OBue1)
ORXIN2-, ORXIN2+	Odd LVDS differential data input(OBlue2-OBlue5, Hsync, Vsync, DE)
ORXCLKIN-, ORXCLKIN+	Odd LVDS differential clock input
ERXIN0-, ERXIN0+	Even LVDS differential data input(ERed0-ERed5, EGreen0)
ERXIN1-, ERXIN1+	Even LVDS differential data input(EGreen1-EGreen5, EBlue0-EBue1)
ERXIN2-, ERXIN2+	Even LVDS differential data input(EBlue2-EBlue5)
ERXCLKIN-, ERXCLKIN+	Even LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

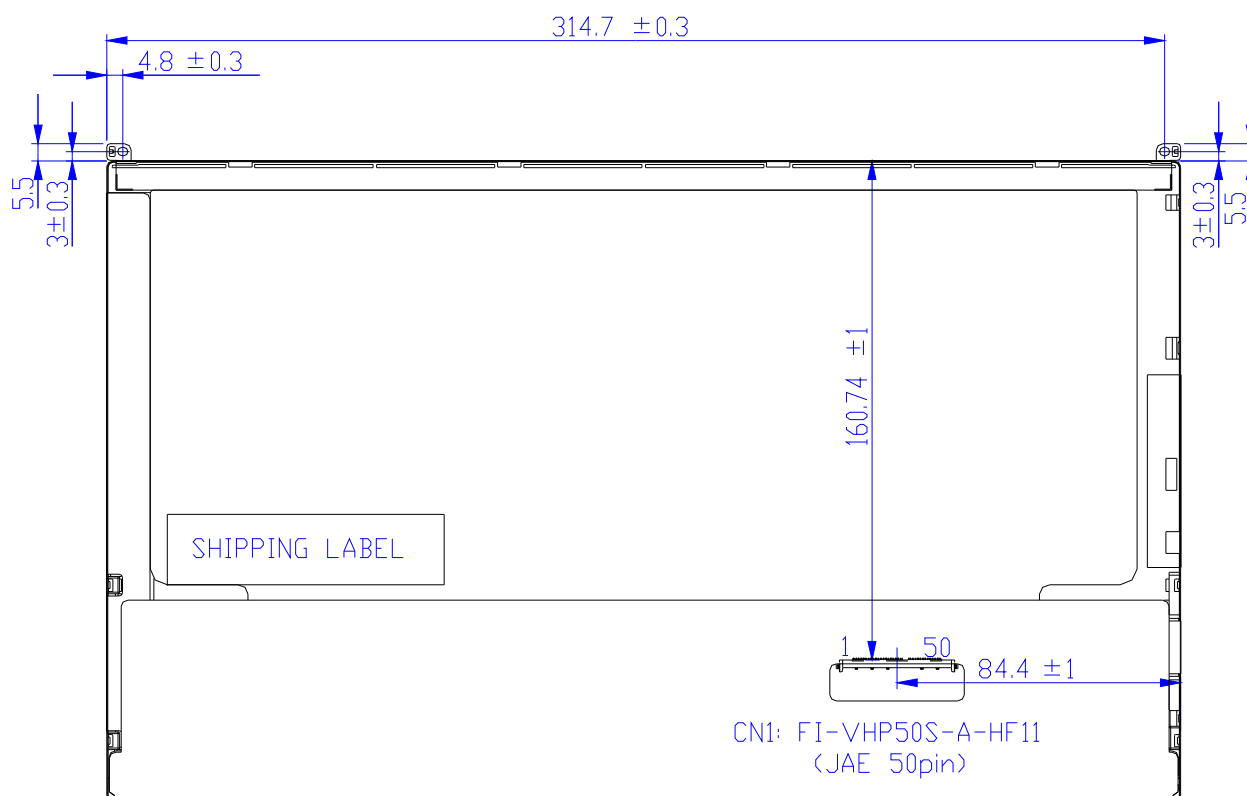
6.3 Integration Interface and Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin No.	Pin Name	Pin Description
1	Test Loop	Test Loop (only to pin 30)
2	VEEDID	EDID 3.3V power
3	VSS	Ground (Panel logic, BL logic)
4	CLK EEDID	EDID clock
5	DATA EEDID	EDID data
6	VSS	Ground (Panel logic, BL logic)
7	Odd_Rin0-	- LVDS differential data input (R0-R5, G0)
8	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0)
9	VSS1	Ground – Shield LVDS Ch1
10	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
11	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	VSS2	Ground – Shield LVDS Ch2
13	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
14	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	VSS3	Ground – Shield LVDS Ch3
16	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
17	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
18	VSS4	Ground – Shield LVDS Ch4
19	Even_Rin0-	- LVDS differential data input (R0-R5, G0) (even pixels)
20	Even_Rin0+	+ LVDS differential data input (R0-R5, G0) (even pixels)
21	VSS5	Ground – Shield LVDS Ch5
22	Even_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (even pixels)
23	Even_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (even pixels)
24	VSS6	Ground – Shield LVDS Ch6
25	Even_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
26	Even_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
27	VSS7	Ground – Shield LVDS Ch7
28	Even_ClkIN-	- LVDS differential clock input (even pixels)
29	Even_ClkIN+	+ LVDS differential clock input (even pixels)
30	Test Loop	Test Loop (only to pin 1)
31	CONNTST	Connector test (this pin connected to pin 50 only) See note 1
32	VDD	Logic power 3.3V (Panel logic, BL logic)
33	VDD	Logic power 3.3V (Panel logic, BL logic)
34	TEST (BIST_EN)	Panel Self Test

35	+5V_ALW	
36	VSS	
37	VSS	
38	PWM_BL	PWM brightness control
39	VBL-	LED power return
40	VBL-	LED power return
41	VBL-	LED power return
42	VBL-	LED power return
43	NC	no connect
44	VBL+	7V - 20V LED power
45	VBL+	7V - 20V LED power
46	VBL+	7V - 20V LED power
47	VBL+	7V - 20V LED power
48	SMB_DATA	SMBus Data
49	SMB_CLK	SMBus Clk
50	CONNTST	Connector test (this pin to be connected to pin 31 only) See note 1

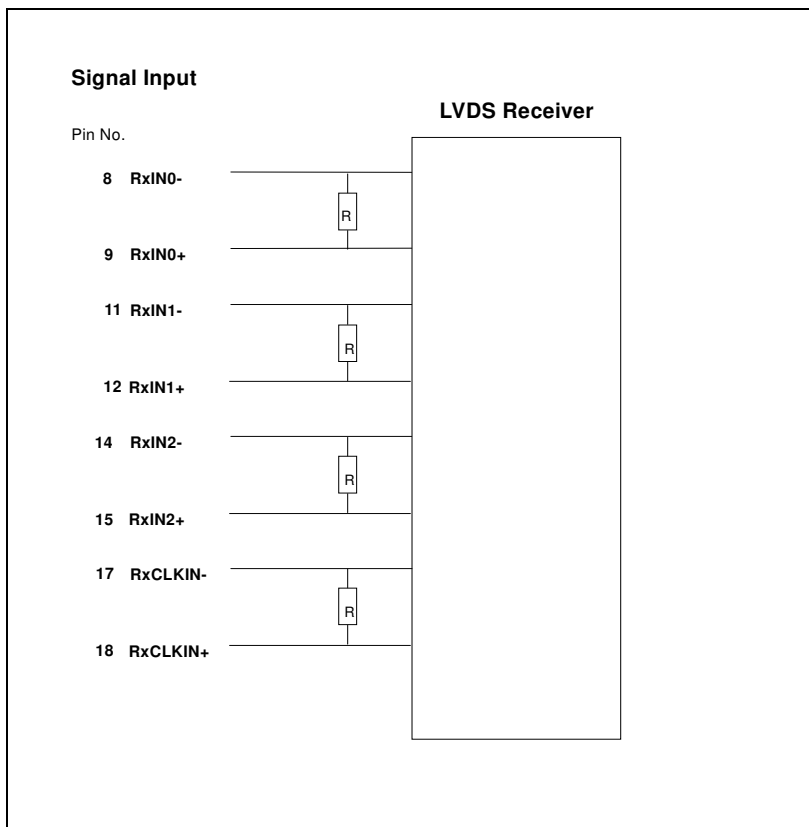
Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

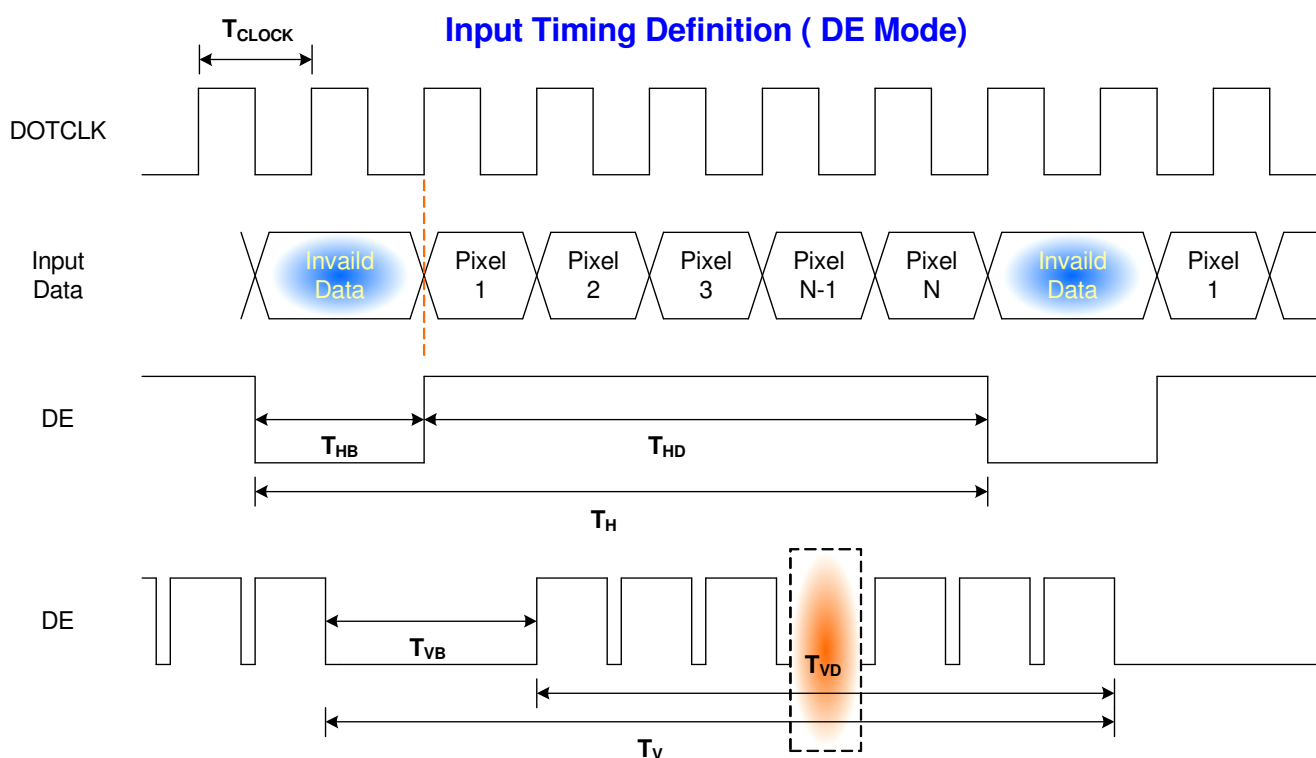
6.4.1 Timing Characteristics

Basically, interface timings should match the 1440x900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$		48.2	60.2	MHz
Vertical Section	Period	T_V	904	912	2048	T_{Line}
	Active	T_{VD}	900	900	900	
	Blanking	T_{VB}	4	12		
Horizontal Section	Period	T_H	760	880	1024	T_{Clock}
	Active	T_{HD}	720	720	720	
	Blanking	T_{HB}	40	160		

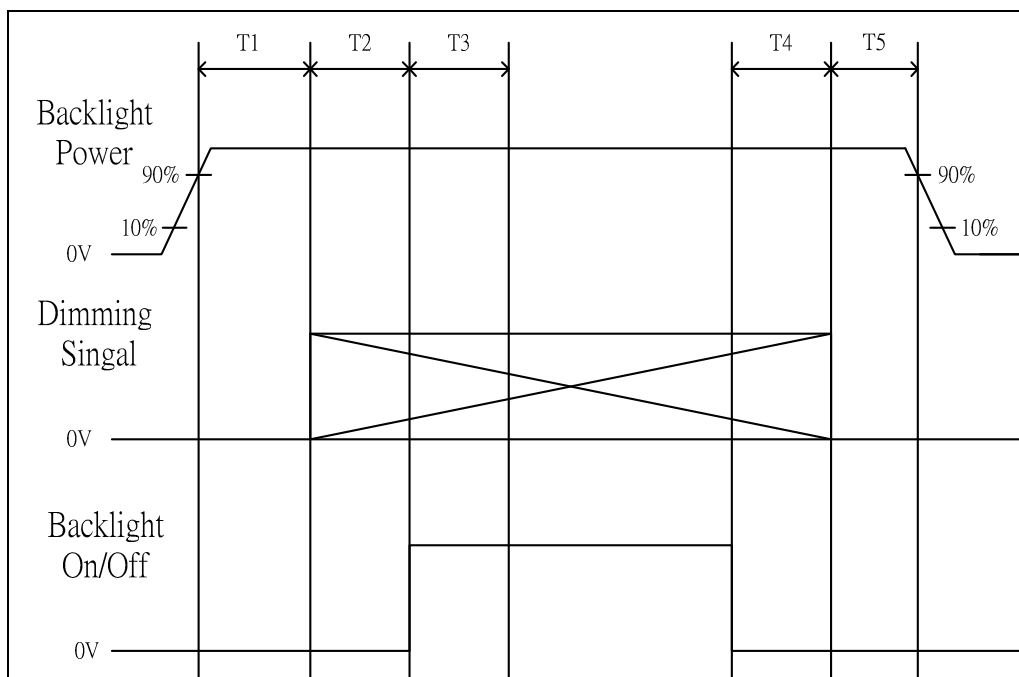
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

LED on/off sequence is as follows. Interface signals are also shown in the chart.



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

Note: The duty of LED dimming signal should be more than 20% in T2 and T3.



7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-VHP50S-A-HF11
Mating Housing/Part Number	FI-VHP50C-A

8. LED Driving Specification

8.1 Connector Description

It is a integrative interface and comibe into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

PIN#	Signal Name	Description
31	CONNTST	Connector test (this pin connected to pin 50 only) See note 1
32	VDD	Logic power 3.3V (Panel logic, BL logic)
33	VDD	Logic power 3.3V (Panel logic, BL logic)
34	TEST (BIST_EN)	Panel Self Test
35	+5V_ALW	
36	VSS	
37	VSS	
38	PWM_BL	PWM brightness control
39	VBL-	LED power return
40	VBL-	LED power return
41	VBL-	LED power return
42	VBL-	LED power return
43	NC	no connect
44	VBL+	7V - 20V LED power
45	VBL+	7V - 20V LED power
46	VBL+	7V - 20V LED power
47	VBL+	7V - 20V LED power
48	SMB_DATA	SMBus Data
49	SMB_CLK	SMBus Clk
50	CONNTST	Connector test (this pin to be connected to pin 31 only) See note 1



9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

10. Reliability

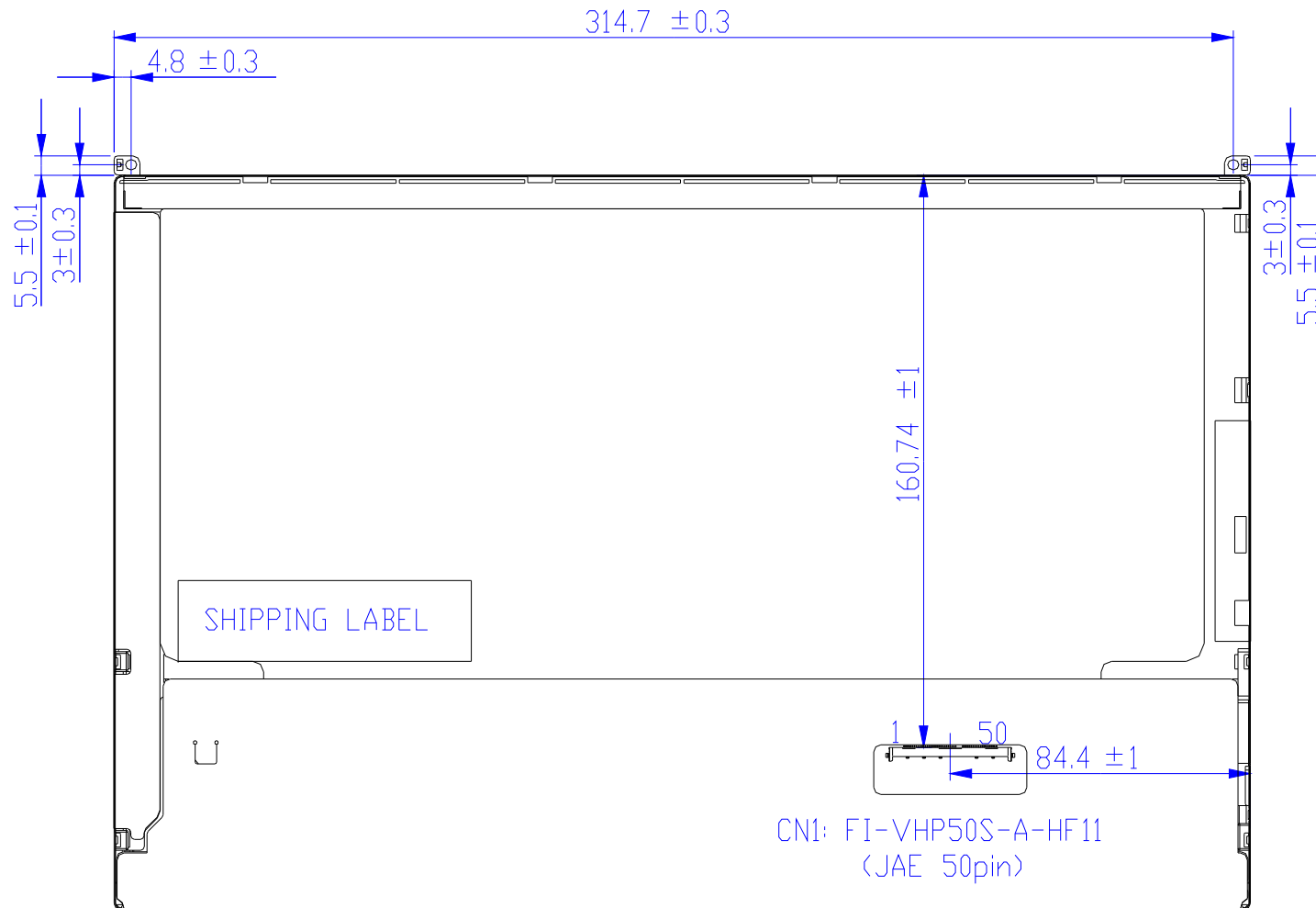
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 95%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 65°C , 20%RH, 300h	
Low Temperature Storage	Ta= -20°C , 50%RH, 300h	
Thermal Shock Test	Ta=-40°C to 65°C , Duration at 30 min, 50 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
. Self-recoverable. No hardware failures.

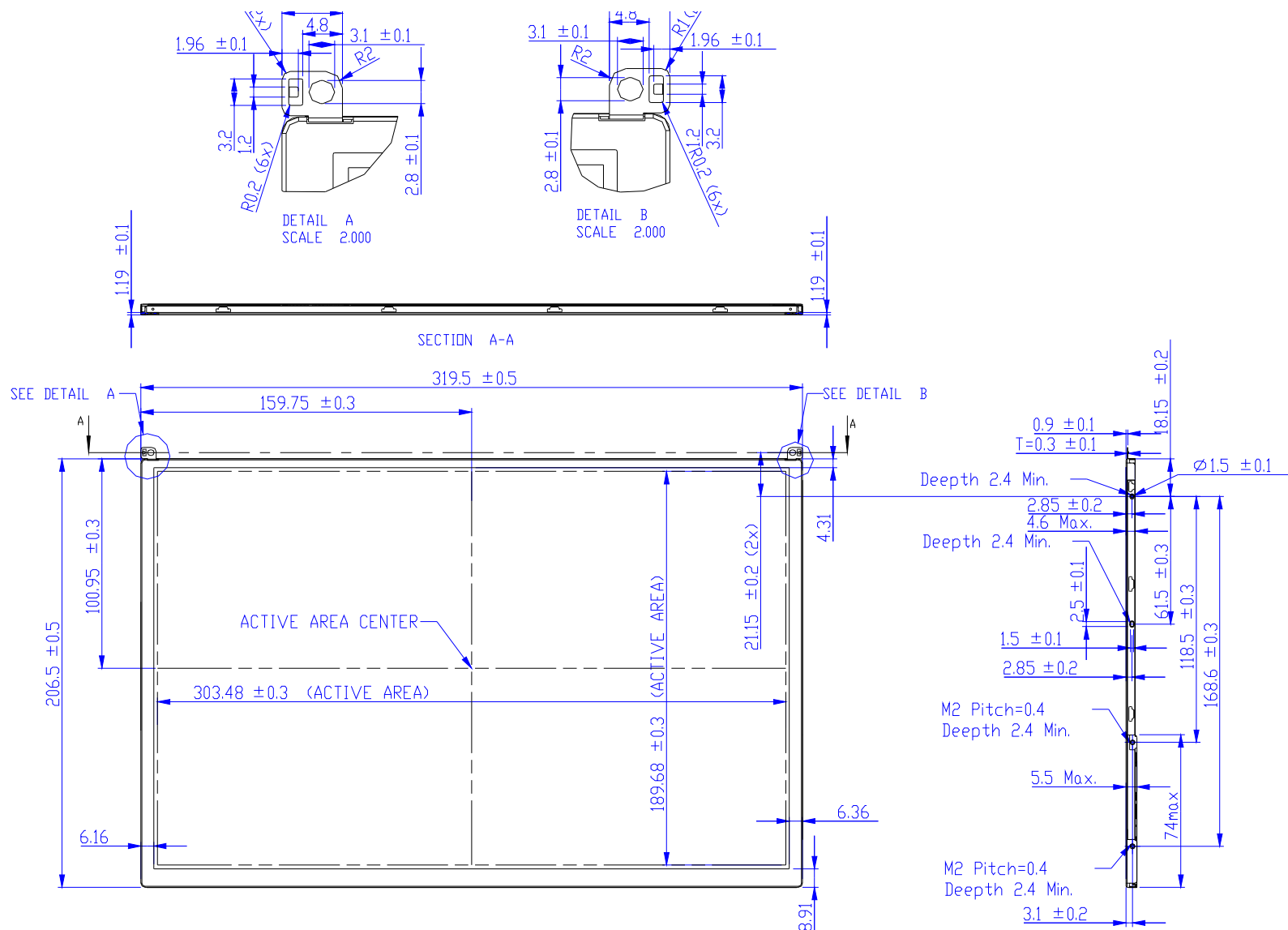
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

11. Mechanical Characteristics

11.1 LCM Outline



Dimension

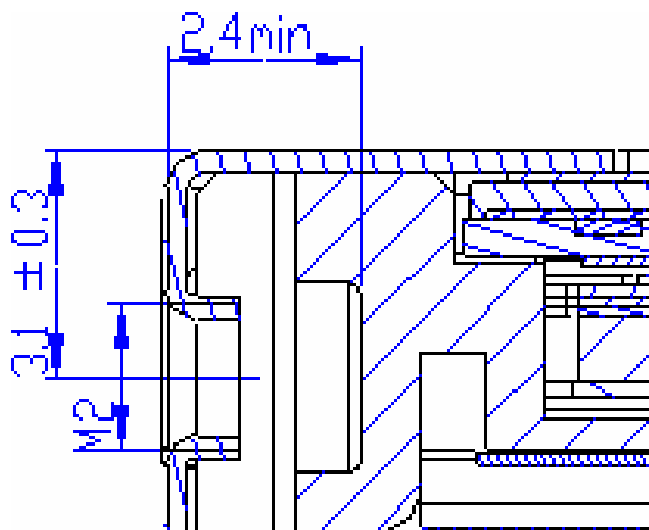


11.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.4 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.3 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm



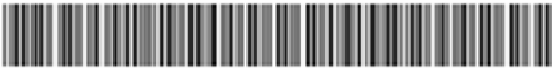
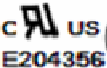


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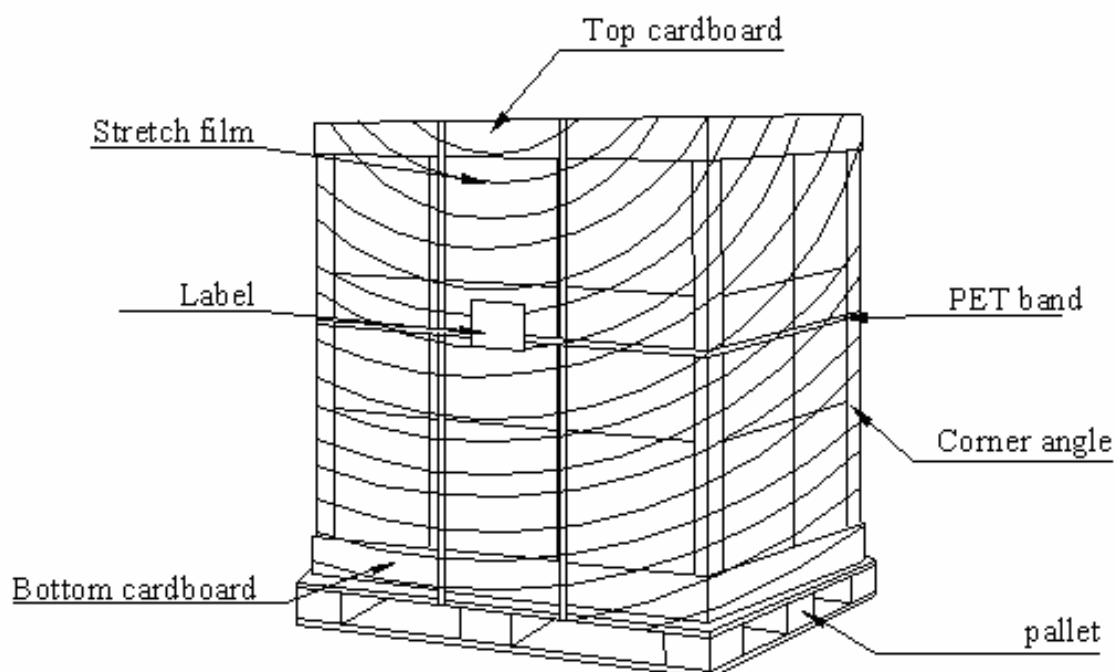
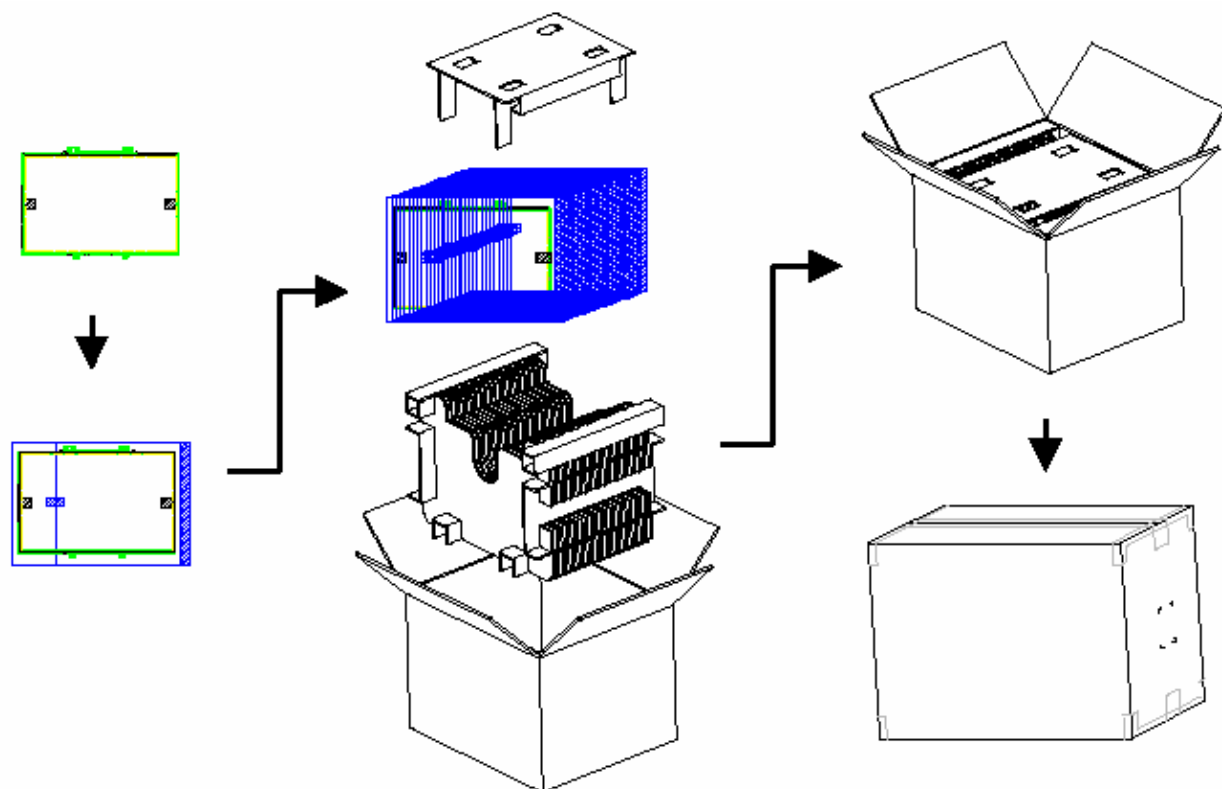
12. Shipping and Package

12.1 Shipping Label Format

 *XXXXXXXXXXXXX.XXXXXX	Manufactured 08/52 Model No: B141PW04 V0 AU Optronics 1A XXG MADE IN CHINA (S01) H/W: 1A F/W:1	   
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12.2 Carton package

The outside dimension of carton is 412 (L)mm x 377 (W)mm x 307 (H)mm





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13. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	47	01000111	71	
0B	hex, LSB first	40	01000000	64	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	12	00010010	18	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input def. (digital I/P, non-TMDS, CRGB)	80	10000000	128	
15	Max H image size (rounded to cm)	1E	00011110	30	
16	Max V image size (rounded to cm)	13	00010011	19	
17	Display Gamma $(=(\text{gamma} \times 100) - 100)$	78	01111000	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	0A	00001010	10	
19	Red/green low bits (Lower 2:2:2:2 bits)	89	10001001	137	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	E5	11100101	229	
1B	Red x (Upper 8 bits)	94	10010100	148	
1C	Red y/ highER 8 bits	57	01010111	87	
1D	Green x	54	01010100	84	
1E	Green y	93	10010011	147	
1F	Blue x	27	00100111	39	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	



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2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	30	00110000	48	
37	Pixel Clock/10000 USB	2A	00101010	42	
38	Horz active Lower 8bits	A0	10100000	160	
39	Horz blanking Lower 8bits	12	00010010	18	
3A	HorzAct:HorzBlnk Upper 4:4 bits	52	01010010	82	
3B	Vertical Active Lower 8bits	84	10000100	132	
3C	Vertical Blanking Lower 8bits	0C	00001100	12	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	40	01000000	64	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	33	00110011	51	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	2F	00101111	47	
43	Vertical Image Size Lower 8bits	BD	10111101	189	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	



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5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	34	00110100	52	4
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	50	01010000	80	P
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	34	00110100	52	4
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	91	10010001	145	