

TFT MONOCHROME LCD MODULE

NL160120AM27-06

NL160120AM27-06A

54 cm (21.3 Type)

UXGA

LVDS Interface (2 ports)

DATA SHEET 

DOD-PD-0975 (1st edition)

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starting to design your system.**

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL160120AM27-06 and NL160120AM27-06A are composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

- Ultra-wide viewing angle (Adoption of Super-Advanced Super Fine TFT (SA-SFT))
- High luminance
- High contrast
- High resolution
- 256 gray scales per 1 sub-pixel (8-bit)
- LVDS interface
- Adjustable gamma characteristics by using built-in 10-bit LUT (look up table)
- Selectable LVDS data input map
- Small foot print
- Incorporated direct light type backlight
- Replaceable inverter
- Difference between NL160120AM27-06 and NL160120AM27-06A

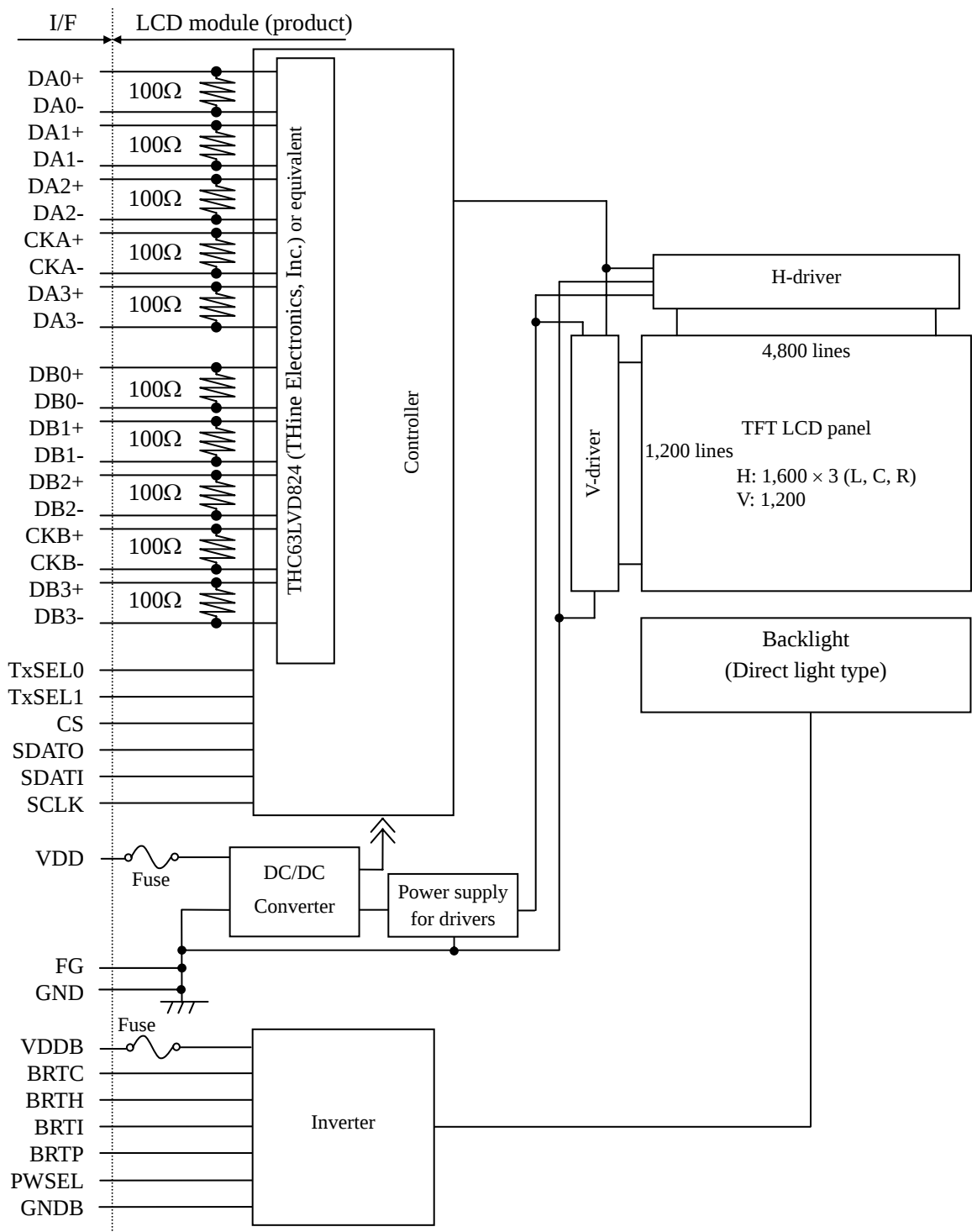
Item	NL160120AM27-06	NL160120AM27-06A
White chromaticity	Wx, Wy = (0.255, 0.310) (typ.)	Wx, Wy = (0.280, 0.304) (typ.)

2. GENERAL SPECIFICATIONS

Display area	432.0 (H) × 324.0 (V) mm	
Diagonal size of display	54 cm (21.3 inches)	
Drive system	a-Si TFT active matrix	
Display grayscale	256 gray scales per 1 sub-pixel (8-bit) (766 gray scales per 1 pixel)	
Pixel	1,600 (H) × 1,200 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)	
Pixel arrangement	LCR vertical stripe	
Dot pitch	0.090 (H) × 0.270 (V) mm	
Pixel pitch	0.270 (H) × 0.270 (V) mm	
Module size	457.0 (W) × 350.0 (H) × 34.0 (D) mm (typ.)	
Weight	2,610 g (typ.)	
Contrast ratio	700:1 (typ.)	
Viewing angle	<i>At the contrast ratio ≥ 10:1</i> • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)	
Designed viewing direction	Viewing angle with optimum grayscale (γ = DICOM): normal axis (perpendicular) Note1	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5400]	
Response time	<i>Ton + Toff (10% ← → 90%)</i> 30 ms (typ.)	
Luminance	<i>At the maximum luminance control</i> 1,800 cd/m ² (typ.)	
White chromaticity	NL160120AM27-06	Wx, Wy = (0.255, 0.310) (typ.)
	NL160120AM27-06A	Wx, Wy = (0.280, 0.304) (typ.)
Signal system	2 ports LVDS interface (THC63LVD824 THine Electronics, Inc. or equivalent) LCR 8-bit signals, Data enable signal (DE), Dot clock (CLK)	
Power supply voltage	LCD panel signal processing board: 12.0V Inverter: 12.0V	
Backlight	Direct light type: 16 cold cathode fluorescent lamps with an inverter { Replaceable part • Inverter: 231PW041 }	
Power consumption	<i>At checkered flag pattern, The maximum luminance control</i> 63.7 W (typ.)	

Note1: When the product luminance is 800cd/m², the gamma characteristic is designed to γ =DICOM.

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and GNDB (Inverter ground) in the product

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±1.0 (W) × 350.0 ±1.0 (H) × 34.0 (typ., D) 36.5 (max. D) Note1, Note2	mm
Display area	432.0 (H) × 324.0 (V) Note1	mm
Weight	2,610 (typ.), 2,800 (max.)	g

Note1: Excluding warpage of the signal processing board cover and the connection board cover

Note2: See "7. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage		LCD panel signal processing board	VDD	-0.3 to +14.0	V	Ta = 25°C
		Inverter	VDDb	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board		Vi	-0.3 to +2.8	V	Ta = 25°C VDD=12.0V
	Inverter	BRTI signal	VBI	-0.3 to +1.5	V	Ta = 25°C VDDb = 12.0V
		B RTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Front surface	TopF	0 to +55	°C	Note1
		Rear surface	TopR	0 to +60	°C	Note2
Relative humidity Note3			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40 < Ta ≤ 50°C
				≤ 70	%	50 < Ta ≤ 55°C
Absolute humidity Note3			AH	≤ 73 Note4	g/m³	Ta > 55°C
Operating altitude			-	≤ 4,850	m	0°C ≤Ta≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C ≤Ta≤ 60°C

Note1: Measured at center of LCD panel surface (including self-heat)

Note2: Measured at center of LCD module's rear shield surface (including self-heat)

Note3: No condensation

Note4: Water amount at Ta = 55°C and RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDD	10.8	12.0	13.2	V	-
Supply current		IDD	-	310 Note1	700 Note2	mA	at VDD=12.0V
Differential input Threshold voltage		VTH	-	-	+100	mV	at VCM=1.2V Note3
		VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	-
Terminating resistance		RT	-	100	-	Ω	-
Control signal input threshold voltage	High	VIH	High must be Open.			-	Note4
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	
Serial communication signal input threshold voltage	High	V+	-	1.4	1.9	V	Note5
	Low	V-	0.4	0.7	-	V	
	Hysteresis	VH	0.3	-	-	V	
Output signal threshold voltage	High	VOH	1.9	-	-	V	Note6
	Low	VOL	-	-	0.4	V	
Output signal current	High	IOH	-4	-	-	mA	
	Low	IOL	-	-	4	mA	

Note1: Checkered flag pattern (by EIAJ ED-2522)

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS driver

Note4: TxSEL0, TxSEL1

Note5: CS, SDAT1, SCLK

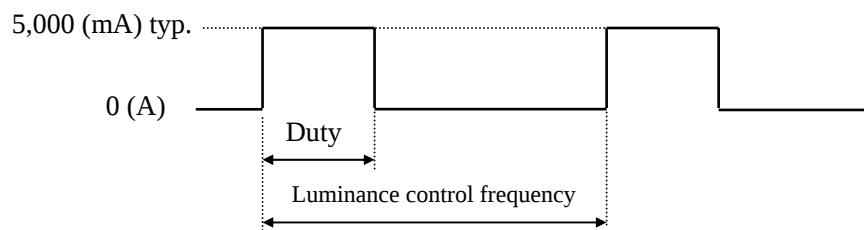
Note6: SDAT0

4.3.2 Inverter

(Ta = 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage			VDDDB	11.4	12.0	12.6	V	-
Power supply current			IDDB	-	5,000	5,700	mA	VDDDB = 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0.25	-	1.0	V	-
	BRTP signal	High	VBPH	2.0	-	5.25	V	
		Low	VBPL	0	-	0.8	V	
	BRTC signal	High	VBCH	2.0	-	5.25	V	
		Low	VBCL	0	-	0.8	V	
	PWSEL signal	High	VBSH	2.0	-	5.25	V	
		Low	VBSL	0	-	0.8	V	
Input current for signals	BRTI signal		IBI	-200	-	1,000	μA	
	BRTP signal	High	IBPH	-	-	1,000	μA	
		Low	IBPL	-600	-	-	μA	
	BRTC signal	High	IBCH	-	-	400	μA	
		Low	IBCL	-600	-	-	μA	
	PWSEL signal	High	IBSH	-	-	440	μA	
		Low	IBSL	-600	-	-	μA	

4.3.3 Inverter current wave



Maximum luminance control: 100%

Minimum luminance control: 20%

Luminance control frequency: 255Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "4.6.2 Detail of BRTP timing".

Note2: The power supply lines (VDDDB and GNDB) have large ripple voltage (See "4.3.4 Power supply voltage ripple".) during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDDB and GNDB) to reduce the noise, if the noise occurred in the circuit..

4.3.4 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1 Unit
VDD	12.0 V	≤ 100	mVp-p
VDDB	12.0 V	≤ 200	mVp-p

Note1: The permissible ripple voltage includes spike noise.

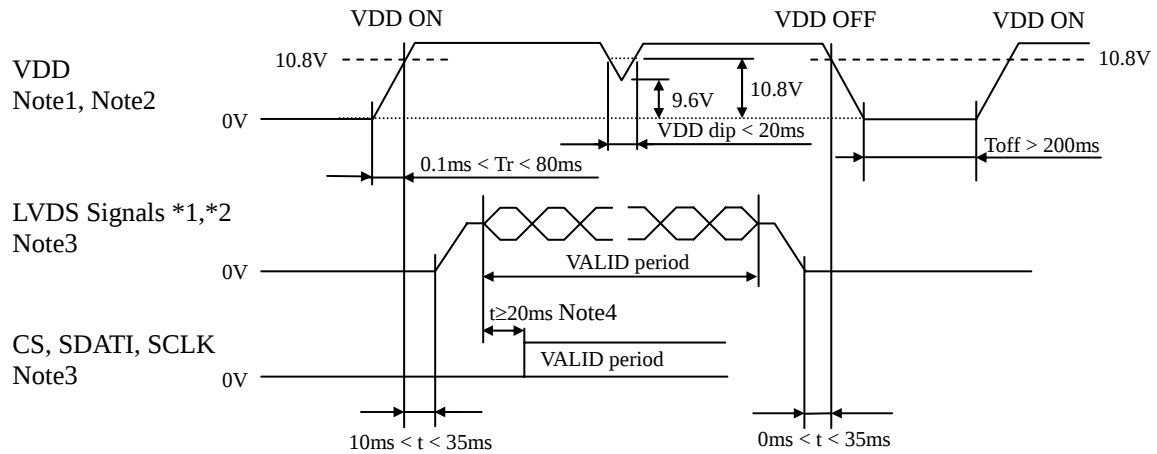
4.3.5 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16132AB	KAMAYA ELECTRIC Co., Ltd.	1.25A	2.5A, 5s max.	Note1
			32V		
VDDB	R451010	Littelfuse Inc.	10A	20A, 5s max.	
			125V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



- *1: LVDS signals: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-
- *2: LVDS signals should be measured at the terminal of 100Ω resistance.

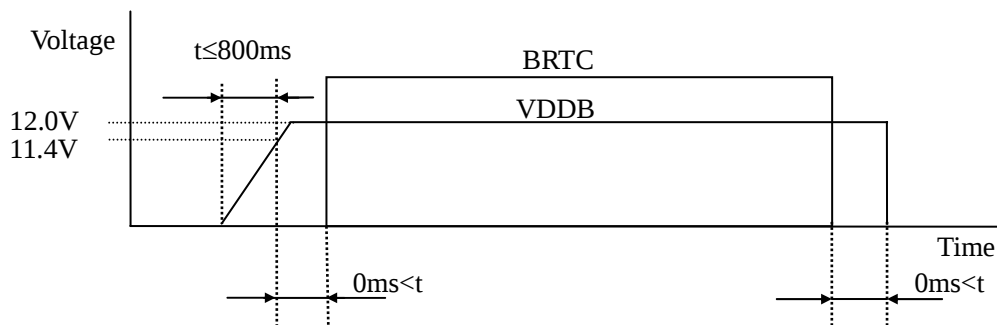
Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: VDD should be 10.8V or more while VDD ON period.

Note3: LVDS signals and CS, SDATI, SCLK must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged. If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VDD.

Note4: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input. When writing and reading the LUT data, see “4.11 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT”.

4.4.2 Inverter



Note1: The inverter power supply voltage (VDDDB) should be inputted within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If t_r is more than 800ms, the backlight will be turned off by a protection circuit for inverter.

Note3: When VDDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

(1) CN1

Socket (LCD module side): DF19G-30P-1H (59/99) (Hirose Electric Co., Ltd. (HRS))

Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd. (HRS))

Pin No.	Symbol	Signal	Remarks					
1	DA0-	Pixel data A0	Odd pixel data Input (LVDS differential signal)		Note1			
2	DA0+							
3	DA1-	Pixel data A1	Odd pixel data Input (LVDS differential signal)		Note1			
4	DA1+							
5	DA2-	Pixel data A2	Odd pixel data Input (LVDS differential signal)		Note1			
6	DA2+							
7	GND	Ground	Signal ground		Note2			
8	CKA-	Pixel clock	Odd pixel clock Input (LVDS differential signal)		Note1			
9	CKA+							
10	DA3-	Pixel data A3	Odd pixel data Input (LVDS differential signal)		Note1			
11	DA3+							
12	DB0-	Pixel data B0	Even pixel data Input (LVDS differential signal)		Note1			
13	DB0+							
14	GND	Ground	Signal ground		Note2			
15	DB1-	Pixel data B1	Even pixel data Input (LVDS differential signal)		Note1			
16	DB1+							
17	GND	Ground	Signal ground		Note2			
18	DB2-	Pixel data B2	Even pixel data Input (LVDS differential signal)		Note1			
19	DB2+							
20	CKB-	Pixel clock	Even pixel clock Input (LVDS differential signal)		Note1			
21	CKB+							
22	DB3-	Pixel data B3	Even pixel data Input (LVDS differential signal)		Note1			
23	DB3+							
24	GND	Ground	Signal ground		Note2			
25	TxSEL0	Selection of LVDS data input map	Note3, Note4	TxSEL1			TxSEL0	Mode
26	TxSEL1			Open	Open	A		
				Open	Low	B		
				Low	Open	C		
				Low	Low	A		
27	GND	Ground	Signal ground					Note2
28	VDD	Power supply	12V					Note2
29	VDD							
30	VDD							

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: This terminal is pulled-up in the product. (Pull-up resistance: 50kΩ)

Note4: See "**4.7 LVDS DATA INPUT MAP**".

(2) CN3

Socket (LCD module side): SM10B-SRSS-TB (J.S.T. Mfg Co., Ltd.)

Adaptable plug: SHR-10V-S, SHR-10V-S-B or 10SR-3S (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	RSVD	Reserved	Keep open
2	RSVD	Reserved	Keep open
3	RSVD	Reserved	Keep open
4	GND	Ground	Signal ground Note1
5	CS	Chip selection	For LUT communication control Note2
6	SDATO	Serial data output	For LUT output signal
7	SDATI	Serial data input	For LUT communication control Note3
8	SCLK	Serial clock	For LUT communication control Note3
9	GND	Ground	Signal ground Note1
10	RSVD	Reserved	Keep open

Note1: All GND terminals should be used without any non-connected lines.

Note2: These terminals are pulled-up in the product. (Pull-up resistance: 50kΩ)

Note3: These terminals are pulled-down in the product. (Pull-down resistance: 50kΩ)

4.5.2 Inverter

CN201 socket (LCD module side): DF3-10P-2H (20/21) (HIROSE ELECTRIC Co.,Ltd.)

Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co.,Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTY (Japan Aviation Electronics Industry Limited (JAE))

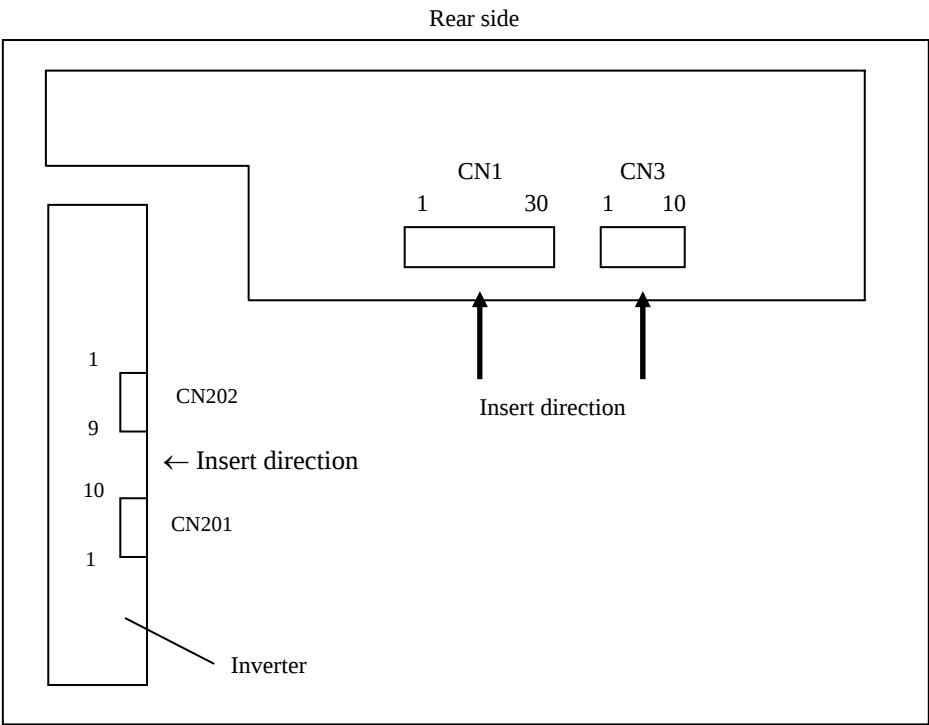
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	See "4.6 LUMINANCE CONTROL".
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	Inverter ground	Note1
9	PWSEL	Selection of luminance control signal method	See "4.6 LUMINANCE CONTROL ". Note2

Note1: All GNDB terminals should be used without any non-connected lines.

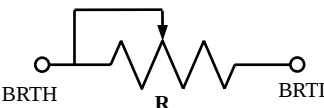
Note2: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket



4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

Method	Adjustment and luminance ratio	PWSEL terminal	B RTP terminal						
Variable resistor control Note1	• Adjustment The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance. The resistor (R) must be connected between BRTH-BRTI terminals.  • Luminance ratio Note3 <table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>1.5 kΩ Note4</td><td>20% (Min. Luminance)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table>	Resistance	Luminance ratio	1.5 kΩ Note4	20% (Min. Luminance)	10 kΩ	100% (Max. Luminance)	High or Open	Open
Resistance	Luminance ratio								
1.5 kΩ Note4	20% (Min. Luminance)								
10 kΩ	100% (Max. Luminance)								
Voltage control Note1	• Adjustment Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance. Luminance is the maximum when BRTI terminal is Open. • Luminance ratio Note3 <table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0.25V Note4</td><td>20% (Min. Luminance)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table>	BRTI Voltage (VBI)	Luminance ratio	0.25V Note4	20% (Min. Luminance)	1.0V	100% (Max. Luminance)		
BRTI Voltage (VBI)	Luminance ratio								
0.25V Note4	20% (Min. Luminance)								
1.0V	100% (Max. Luminance)								
Pulse width modulation Note1 Note2 Note5	• Adjustment Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (B RTP signal) is input into B RTP terminal. The luminance is controlled by duty ratio of B RTP signal. • Luminance ratio Note3 <table><tr><th>Duty ratio Note4</th><th>Luminance ratio</th></tr><tr><td>0.2</td><td>20% (Min. Luminance)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table>	Duty ratio Note4	Luminance ratio	0.2	20% (Min. Luminance)	1.0	100% (Max. Luminance)	Low	B RTP signal
Duty ratio Note4	Luminance ratio								
0.2	20% (Min. Luminance)								
1.0	100% (Max. Luminance)								

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: The inverter will stop working, when B RTP signal is fixed to Low while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if B RTP signal is input again. This is not out of order. Backlight inverter will start to work when power is supplied again.

Note3: These data are the target values.

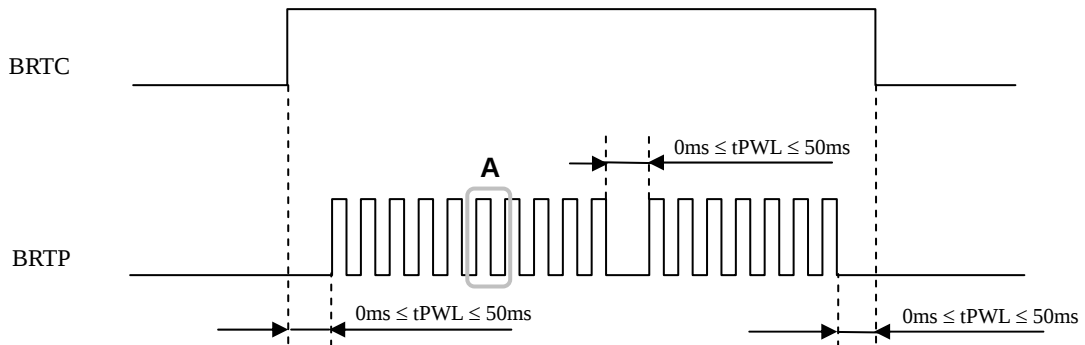
Note4: Do not set the variable resistor and BRTI voltage in less than 1.5k Ω or less than 0.25V. Otherwise flicker or display mura may cause, or the lamp may not be turned on.

Note5: See "4.6.2 Detail of B RTP timing".

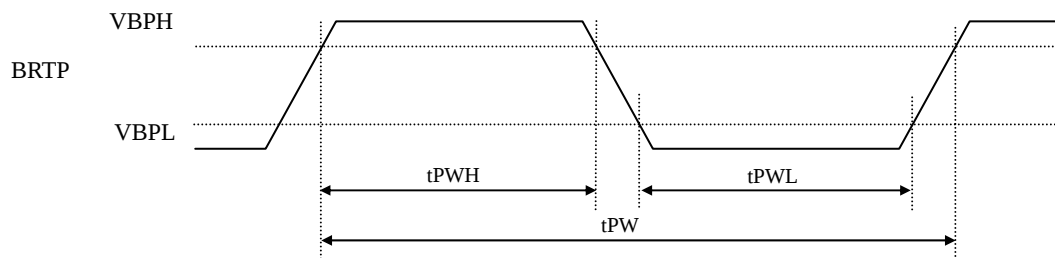
4.6.2 Detail of B RTP timing

(1) Timing diagrams

• Outline chart



• Detail of A part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	185	-	325	Hz	Note1, Note2
Duty ratio	DL	0.2	-	1.0	-	Note1, Note3
Low period	tPWL	0	-	50	ms	Note4

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW} \quad DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.

$$\text{Luminance control frequency} = 1/tv \times (n+0.25) \text{ [or } (n + 0.75)]$$

$$n = 1, 2, 3 \dots \dots$$

tv: Vertical cycle (See "4.9.1 Timing characteristics".)

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "4.6.1 Luminance control methods".

Note4: If tPWL is more than 50ms, the backlight will be turned off by a protection circuit for inverter.

4.7 LVDS DATA INPUT MAP

4.7.1 Mode A

Input data		Transmitter				CN1	
		Pin	THC63LVDF83A	Pin	THC63LVD823	Pin	Symbol
Odd pixel data and control signal	LA2	→	51	TA0	53	R12	
	LA3	→	52	TA1	54	R13	TA1- → 1 DA0-
	LA4	→	54	TA2	57	R14	TA1+ → 2 DA0+
	LA5	→	55	TA3	58	R15	
	LA6	→	56	TA4	59	R16	TB1- → 3 DA1-
	LA7	→	3	TA5	60	R17	TB1+ → 4 DA1+
	CA2	→	4	TA6	63	G12	
	CA3	→	6	TB0	64	G13	TC1- → 5 DA2-
	CA4	→	7	TB1	65	G14	TC1+ → 6 DA2+
	CA5	→	11	TB2	66	G15	7 GND
	CA6	→	12	TB3	67	G16	TCLK1- → 8 CKA-
	CA7	→	14	TB4	68	G17	TCLK1+ → 9 CKA+
	RA2	→	15	TB5	73	B12	
	RA3	→	19	TB6	74	B13	TD1- → 10 DA3-
	RA4	→	20	TC0	75	B14	TD1+ → 11 DA3+
	RA5	→	22	TC1	76	B15	
	RA6	→	23	TC2	77	B16	
	RA7	→	24	TC3	78	B17	
	Note3 RSVD	→	27	TC4	7	RSVD	
	Note3 RSVD	→	28	TC5	8	RSVD	
	DE	→	30	TC6	9	DE	
	LA0	→	50	TD0	51	R10	
	LA1	→	2	TD1	52	R11	
	CA0	→	8	TD2	61	G10	
	CA1	→	10	TD3	62	G11	
	RA0	→	16	TD4	69	B10	
	RA1	→	18	TD5	70	B11	
	Note1 RSVD	→	25	TD6	-		
	CLK	→	31	CLKIN	10	CLK	
Even pixel data	LB2	→	51	TA0	81	R22	
	LB3	→	52	TA1	82	R23	TA2- → 12 DB0-
	LB4	→	54	TA2	83	R24	TA2+ → 13 DB0+
	LB5	→	55	TA3	84	R25	14 GND
	LB6	→	56	TA4	85	R26	TB2- → 15 DB1-
	LB7	→	3	TA5	86	R27	TB2+ → 16 DB1+
	CB2	→	4	TA6	91	G22	17 GND
	CB3	→	6	TB0	92	G23	TC2- → 18 DB2-
	CB4	→	7	TB1	93	G24	TC2+ → 19 DB2+
	CB5	→	11	TB2	94	G25	
	CB6	→	12	TB3	95	G26	TCLK2- → 20 CKB-
	CB7	→	14	TB4	96	G27	TCLK2+ → 21 CKB+
	RB2	→	15	TB5	99	B22	
	RB3	→	19	TB6	100	B23	TD2- → 22 DB3-
	RB4	→	20	TC0	1	B24	TD2+ → 23 DB3+
	RB5	→	22	TC1	2	B25	24 GND
	RB6	→	23	TC2	5	B26	25 TxSEL0
	RB7	→	24	TC3	6	B27	26 TxSEL1
	Note3 RSVD	→	27	TC4	-		27 GND
	Note3 RSVD	→	28	TC5	-		28 VDD
	Note3 RSVD	→	30	TC6	-		29 VDD
	LB0	→	50	TD0	79	R20	30 VDD
	LB1	→	2	TD1	80	R21	
	CB0	→	8	TD2	89	G20	
	CB1	→	10	TD3	90	G21	
	RB0	→	16	TD4	97	B20	
	RB1	→	18	TD5	98	B21	
	Note3 RSVD	→	25	TD6	-		
	CLK	→	31	CLKIN	-		

4.7.2 Mode B

Input data		Transmitter		CN1	
Note1		Pin	DS90CF383, C385	Pin	Symbol
Odd pixel data and control signal	LA7	→	51 TXIN0	Note2	1 DA0-
	LA6	→	52 TXIN1		2 DA0+
	LA5	→	54 TXIN2		
	LA4	→	55 TXIN3		
	LA3	→	56 TXIN4		3 DA1-
	LA2	→	3 TXIN6		4 DA1+
	CA7	→	4 TXIN7		
	CA6	→	6 TXIN8		5 DA2-
	CA5	→	7 TXIN9		6 DA2+
	CA4	→	11 TXIN12		7 GND
	CA3	→	12 TXIN13		8 CKA-
	CA2	→	14 TXIN14		9 CKA+
	RA7	→	15 TXIN15		
	RA6	→	19 TXIN18		10 DA3-
	RA5	→	20 TXIN19		11 DA3+
	RA4	→	22 TXIN20		
	RA3	→	23 TXIN21		
	RA2	→	24 TXIN22		
	Note3 RSVD	→	27 TXIN24		
	Note3 RSVD	→	28 TXIN25		
	DE	→	30 TXIN26		
	LA1	→	50 TXIN27		
	LA0	→	2 TXIN5		
	CA1	→	8 TXIN10		
	CA0	→	10 TXIN11		
	RA1	→	16 TXIN16		
	RA0	→	18 TXIN17		
	Note3 RSVD	→	25 TXIN23		
	CLK	→	31 CLKIN		
Even pixel data	LB7	→	51 TXIN0	Note2	12 DB0-
	LB6	→	52 TXIN1		13 DB0+
	LB5	→	54 TXIN2		14 GND
	LB4	→	55 TXIN3		
	LB3	→	56 TXIN4		15 DB1-
	LB2	→	3 TXIN6		16 DB1+
	CB7	→	4 TXIN7		17 GND
	CB6	→	6 TXIN8		18 DB2-
	CB5	→	7 TXIN9		19 DB2+
	CB4	→	11 TXIN12		
	CB3	→	12 TXIN13		20 CKB-
	CB2	→	14 TXIN14		21 CKB+
	RB7	→	15 TXIN15		
	RB6	→	19 TXIN18		22 DB3-
	RB5	→	20 TXIN19		23 DB3+
	RB4	→	22 TXIN20		24 GND
	RB3	→	23 TXIN21		25 TxSEL0
	RB2	→	24 TXIN22		26 TxSEL1
	Note3 RSVD	→	27 TXIN24		27 GND
	Note3 RSVD	→	28 TXIN25		28 VDD
	Note3 RSVD	→	30 TXIN26		29 VDD
	LB1	→	50 TXIN27		30 VDD
	LB0	→	2 TXIN5		
	CB1	→	8 TXIN10		
	CB0	→	10 TXIN11		
	RB1	→	16 TXIN16		
	RB0	→	18 TXIN18		
	Note3 RSVD	→	25 TXIN23		
	CLK	→	31 CLKIN		

4.7.3 Mode C

Input data		Transmitter		CN1	
Note1		Pin	DS90CF383, C385	Pin	Symbol
Odd pixel data and control signal	LA0	→	51 TXIN0	Note2	1 DA0-
	LA1	→	52 TXIN1		2 DA0+
	LA2	→	54 TXIN2		3 DA1-
	LA3	→	55 TXIN3		4 DA1+
	LA4	→	56 TXIN4		5 DA2-
	LA5	→	3 TXIN6		6 DA2+
	CA0	→	4 TXIN7		7 GND
	CA1	→	6 TXIN8		8 CKA-
	CA2	→	7 TXIN9		9 CKA+
	CA3	→	11 TXIN12		10 DA3-
	CA4	→	12 TXIN13		11 DA3+
	CA5	→	14 TXIN14		
	RA0	→	15 TXIN15		
	RA1	→	19 TXIN18		
	RA2	→	20 TXIN19		
	RA3	→	22 TXIN20		
	RA4	→	23 TXIN21		
	RA5	→	24 TXIN22		
	Note3 RSVD	→	27 TXIN24		
	Note3 RSVD	→	28 TXIN25		
	DE	→	30 TXIN26		
	LA6	→	50 TXIN27		
	LA7	→	2 TXIN5		
	CA6	→	8 TXIN10		
	CA7	→	10 TXIN11		
	RA6	→	16 TXIN16		
	RA7	→	18 TXIN17		
	Note3 RSVD	→	25 TXIN23		
	CLK	→	31 CLKIN		
Even pixel data	LB0	→	51 TXIN0	Note2	12 DB0-
	LB1	→	52 TXIN1		13 DB0+
	LB2	→	54 TXIN2		14 GND
	LB3	→	55 TXIN3		15 DB1-
	LB4	→	56 TXIN4		16 DB1+
	LB5	→	3 TXIN6		17 GND
	CB0	→	4 TXIN7		18 DB2-
	CB1	→	6 TXIN8		19 DB2+
	CB2	→	7 TXIN9		20 CKB-
	CB3	→	11 TXIN12		21 CKB+
	CB4	→	12 TXIN13		22 DB3-
	CB5	→	14 TXIN14		23 DB3+
	RB0	→	15 TXIN15		24 GND
	RB1	→	19 TXIN18		25 TxSEL0
	RB2	→	20 TXIN19		26 TxSEL1
	RB3	→	22 TXIN20		27 GND
	RB4	→	23 TXIN21		28 VDD
	RB5	→	24 TXIN22		29 VDD
	Note3 RSVD	→	27 TXIN24		30 VDD
	Note3 RSVD	→	28 TXIN25		
	Note3 RSVD	→	30 TXIN26		
	LB6	→	50 TXIN27		
	LB7	→	2 TXIN5		
	CB6	→	8 TXIN10		
	CB7	→	10 TXIN11		
	RB6	→	16 TXIN16		
	RB7	→	18 TXIN18		
	Note3 RSVD	→	25 TXIN23		
	CLK	→	31 CLKIN		

Note1: LSB (Least Significant Bit) – LA0, CA0, RA0, LB0, CB0, RB0

MSB (Most Significant Bit) – LA7, CA7, RA7, LB7, CB7, RB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

4.8 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display 256 gray scales in each LCR sub-pixel and 766 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display grayscale		Data signal (0: Low level, 1: High level)																							
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	↑					:								:							:				
	↓					:								:							:				
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	↑					:								:							:				
	↓					:								:							:				
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
	↑					:								:							:				
	↓					:								:							:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
Left sub-pixel gray scale		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.9 INPUT SIGNAL TIMINGS

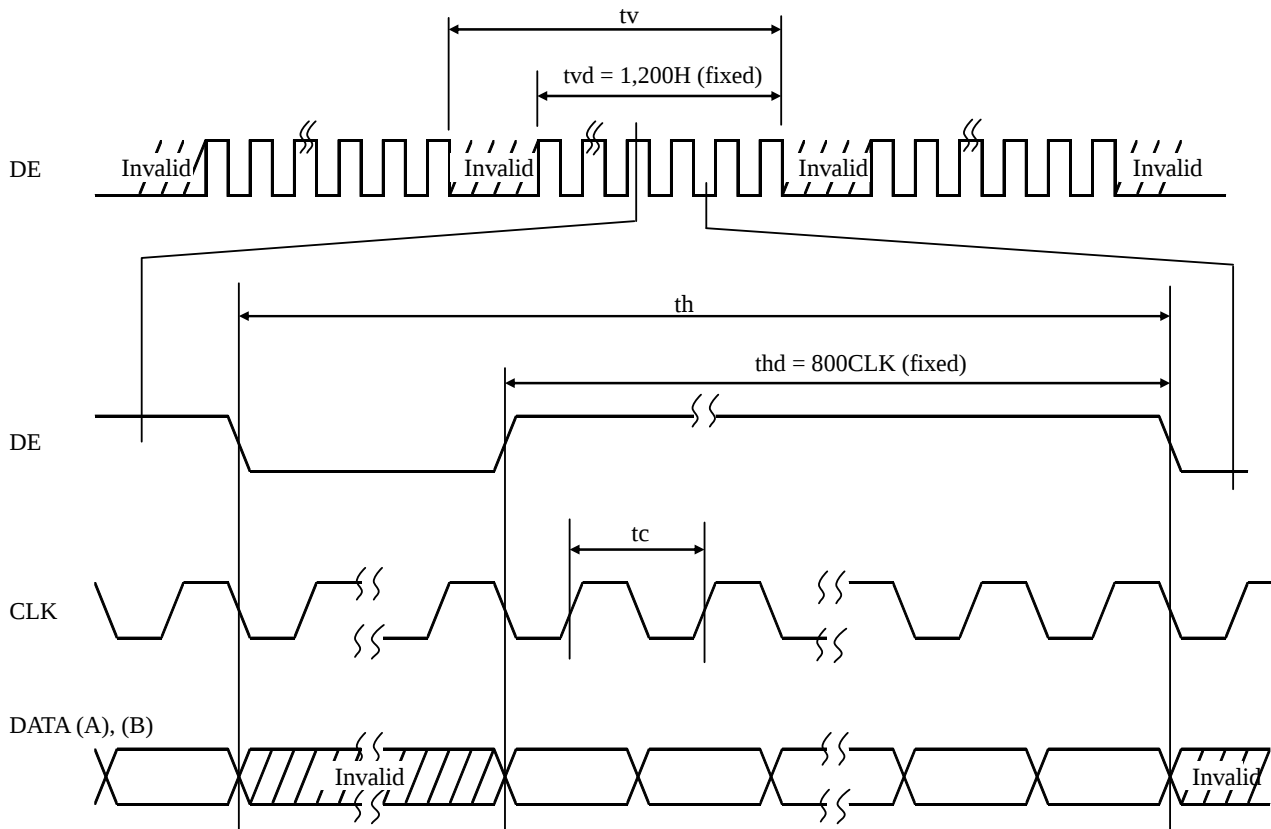
4.9.1 Timing characteristics

	Parameter	Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	1/ tc	60.0	64.5	65.0	MHz	LVDS transmitter input
	Pulse width	tc	15.38	15.5	-	ns	
	Duty	-	See the data sheet of LVDS transmitter.			-	-
	Rise, fall	-				ns	
Horizontal	Cycle period	th	13.1	13.3	19.2	μs	Note1
			848	860	1,156	CLK	
	Display period	thd	800			CLK	-
Vertical	Cycle period	1/tv	59	60	61	Hz	-
		tv	1,206	1,250	-	H	
	Display period	tvd	1,200			H	-
DE, DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
	Hold time	-				ns	
	Rise, fall	-				ns	

Note1: During operation, fluctuation of horizontal cycle period must not exceed ± 1 CLK. Otherwise function errors will occur in LCD module.

e.g.: Acceptable fluctuation range is 1,079-1,081 CLK, when the horizontal cycle period is 1,080 CLK.

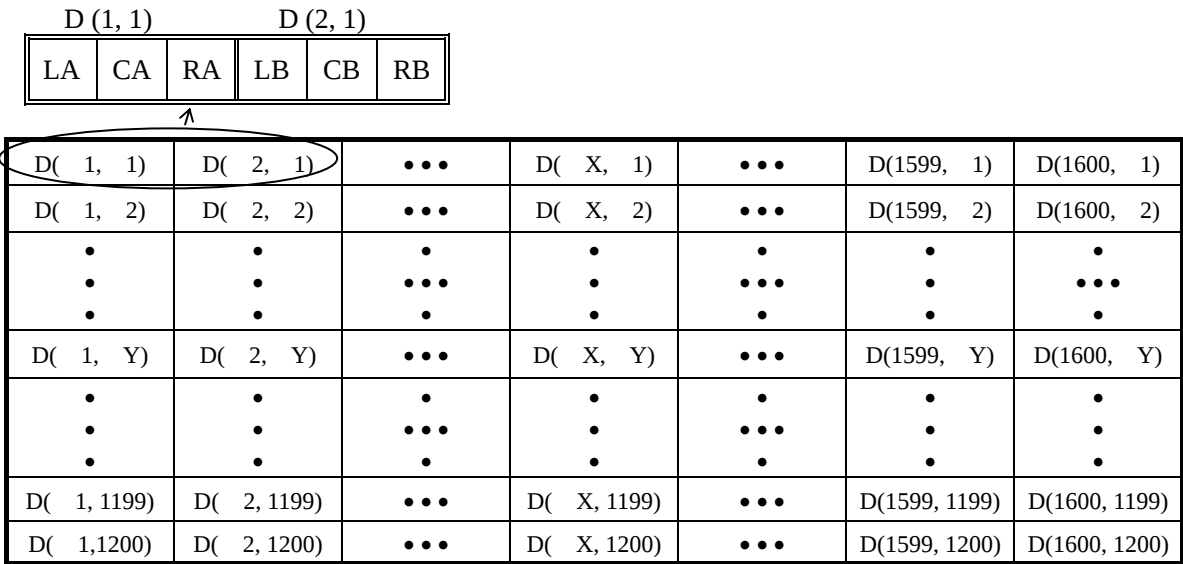
4.9.2 Input signal timing chart



4.10 DISPLAY POSITIONS

Odd pixel: LA= Left data
 CA= Center data
 RA= Right data

Even pixel: LB= Left data
 CB= Center data
 RB= Right data



4.11 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics for each 8-bit LCR data is possible by using built-in 10-bit LUT (look up table) for Gamma characteristics.

The LUT is set with the serial data. The combination of the control command determines the R/W actions.: READ, Random/Sequential Address WRITE and Individual/Simultaneous LCR setting.

The serial data is composed as Table1.

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See Table2 and 3.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See Table4.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	
D15	Dummy	Dummy Data "0"	See Table5.
D14	Dummy	Dummy Data "0"	
D13	Dummy	Dummy Data "0"	
D12	Dummy	Dummy Data "0"	
D11	Dummy	Dummy Data "0"	
D10	Dummy	Dummy Data "0"	
D9	DATA9	LUT Data (MSB)	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

Table2: Command table (CMD5 to CMD0: 6-bit)

DATA name	Parameter	Remarks
CMD5	Selection of WRITE/READ mode "1": WRITE mode "0": READ mode	In case of "0", must be set as follows. CMD4: "1", CMD3: "0", CMD2: "1" CMD1: "0", CMD0: "0"
CMD4	Must be set to "1".	-
CMD3	Selection of Random/Sequential Address WRITE "1": Random Address WRITE "0": Sequential Address WRITE	-
CMD2	Must be set to "1".	-
CMD1	Selection of Individual/Simultaneous LCR setting "1": Individual LCR setting "0": Simultaneous LCR setting	"1": Select the sub-pixel by using ADD9 and ADD8. (See Table4.) "0": ADD9 and ADD8 are invalid.
CMD0	Must be set to "0".	-

Table3: Command Combination table (CMD5 to CMD0: 6-bit)

CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Mode
1	1	1	1	1	0	Random Address WRITE, Individual LCR setting
1	1	1	1	0	0	Random Address WRITE, Simultaneous LCR setting
1	1	0	1	1	0	Sequential Address WRITE, Individual LCR setting
1	1	0	1	0	0	Sequential Address WRITE, Simultaneous LCR setting
0	1	0	1	0	0	READ mode

*Another combinations are prohibited, and may cause function error.

Table4: Address table (ADD9 to ADD0: 10-bit)

DATA name	Parameter	Remarks
ADD9	Sub-pixel selection ADD[9:8]= 0:0 Left sub-pixel 0:1 Center sub-pixel 1:0 Right sub-pixel 1:1 ON/OFF selection of Gamma Correction	When "ADD[9:8]=1:1", ON/OFF of Gamma correction can select according to the GMA[2:0]. (See Table6 and Table7.)
ADD8		
ADD7		
ADD6		
ADD5	LUT Address 256 address = 00h - FFh	When ADD[9:8] = 1:1, ADD[7:0] must be set to 00h.
ADD4		
ADD3		
ADD2		
ADD1		
ADD0		

Table5: Data table (DATA15 to DATA0: 16-bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	DATA9	[MSB] 10-bit LUT Data 000h - 3FFh [LSB]	-
DATA8	DATA8		
DATA7	DATA7		
DATA6	DATA6		
DATA5	DATA5		
DATA4	DATA4		
DATA3	DATA3		
DATA2	DATA2		
DATA1	DATA1		
DATA0	DATA0		

Table6: Gamma correction table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	Dummy		
DATA8	Dummy		
DATA7	Dummy		
DATA6	Dummy		
DATA5	Dummy		
DATA4	Dummy		
DATA3	Dummy		
DATA2	GMA2	[MSB]	See Table7.
DATA1	GMA1	GMA Data	
DATA0	GMA0	[LSB]	

Table7: Control code GMA[2:0]

GMA2	GMA1	GMA0	Function
0	0	0	No correction (Initial setting)
0	0	1	Correction according to the LUT Data. Note1

*Another combinations are prohibited, and may cause function error.

Note1: Initial setting of the LUT is undefined data. The LUT should be enabled by setting of the GMA after writing the LUT data in all the 256 addresses, in order to avoid undefined data display.

Note2: Transfer the data every power-on, because the LUT data isn't stored in the LCD module.

Note3: When writing and reading the LUT data, a noise may appear on the display image. In order to prevent the noise appearing on the display, following measures should be performed.

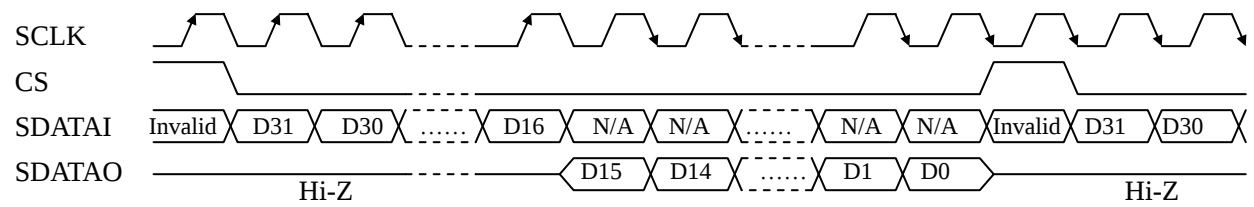
(1)The LUT data should be rewritten during invalid period of pixel data (See "**4.9 INPUT SIGNAL TIMINGS**").).

(2)The LUT data should be rewritten while the LUT data is invalid.

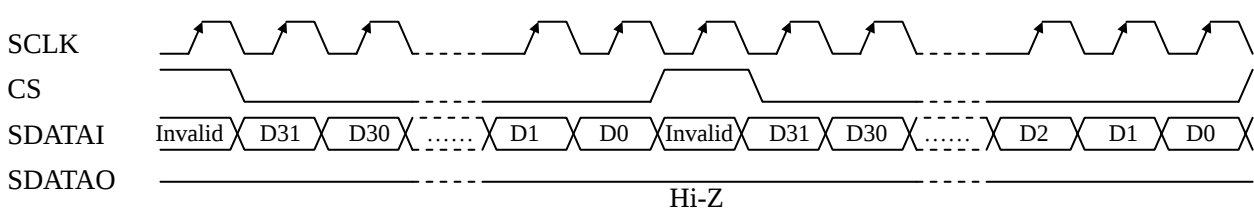
4.12 LUT SERIAL COMMUCATION TIMINGS

4.12.1 Timing Chart

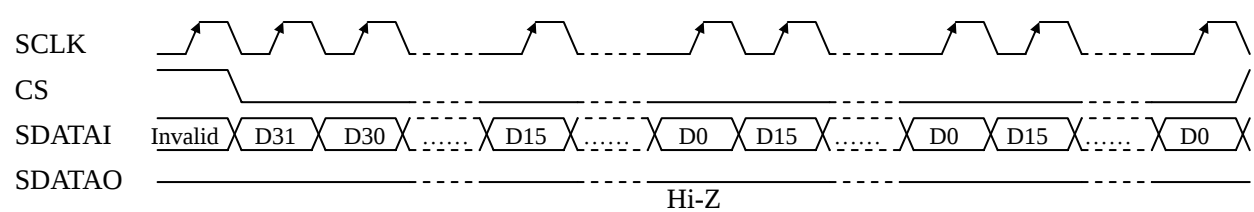
(1) READ Timing Chart



(2) Random Address WRITE Timing Chart



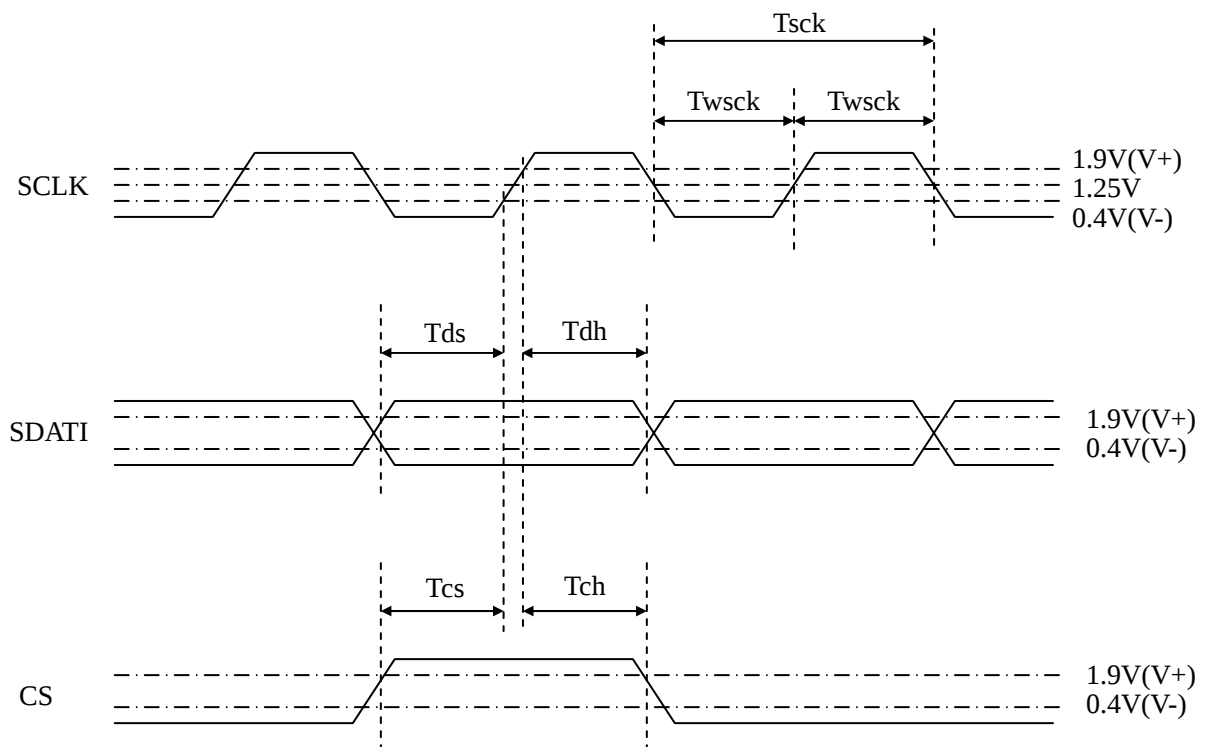
(3) Sequential Address WRITE Timing Chart



4.12.2 Timing specifications

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
SCLK Frequency	1/Tsck	-	-	5	MHz	-
SCLK Pulse Width (WRITE)	Twscck	50	-	-	ns	-
SCLK Pulse Width (READ)	Twscck	5	-	-	tc	Note1
SDATI-SCLK Setup Time	Tds	50	-	-	ns	-
SDATI-SCLK Hold Time	Tdh	50	-	-	ns	-
CS-SCLK Setup Time	Tcs	50	-	-	ns	-
CS-SCLK Hold Time	Tch	50	-	-	ns	-

Note1: At the READ of the serial communication mode, the SCLK Pulse Width (Twscck) must be greater than 5CLK (5 tc's). (See "4.9.1 Timing characteristics".)



Note2: During the serial communication mode, the display noise may appear because of rewriting the data. To avoid this, rewrite the data in the blanking timing. The external noise may cause the data change, refresh the data regularly according to need.

4.13 OPTICS

4.13.1 Optical characteristics

(1) NL160120AM27-06

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	1,400	1,800	-	cd/m ²	BM-5A or SR-3	-
Contrast ratio		White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	400	700	-	-	BM-5A or SR-3	Note3
Luminance uniformity		White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.2	1.3	-	BM-5A	Note4
Chromaticity	White	x coordinate	Wx	-	0.255	-	-	SR-3	Note5
		y coordinate	Wy	-	0.310	-	-		
Response time		Black to White	Ton	-	15	25	ms	BM-5A	Note6 Note7
		White to Black	Toff	-	15	25	ms		
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θR	70	85	-	°	BM-5A	Note8
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θL	70	85	-	°		
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θU	70	85	-	°		
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θD	70	85	-	°		

(2) NL160120AM27-06A

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	1,400	1,800	-	cd/m ²	BM-5A or SR-3	-
Contrast ratio		White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	400	700	-	-	BM-5A or SR-3	Note3
Luminance uniformity		White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.2	1.3	-	BM-5A	Note4
Chromaticity	White	x coordinate	Wx	-	0.280	-	-	SR-3	Note5
		y coordinate	Wy	-	0.304	-	-		
Response time		Black to White	Ton	-	15	25	ms	BM-5A	Note6
		White to Black	Toff	-	15	25	ms		Note7
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θR	70	85	-	°	BM-5A	Note8
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θL	70	85	-	°		
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θU	70	85	-	°		
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θD	70	85	-	°		

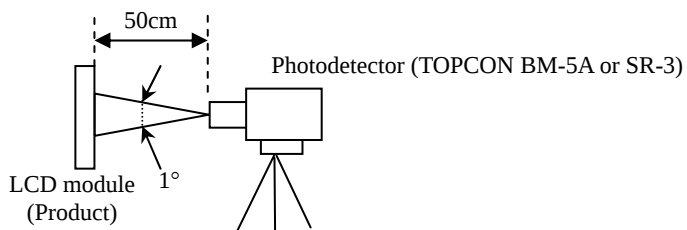
Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 12.0V, VDDB = 12.0V, Luminance control = maximum,

Display mode: UXGA, Horizontal cycle = 1/75 kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note3: See "**4.13.2 Definition of contrast ratio**".

Note4: See "**4.13.3 Definition of luminance uniformity**".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = 36°C

Note7: See "**4.13.4 Definition of response times**".

Note8: See "**4.13.5 Definition of viewing angles**".

4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

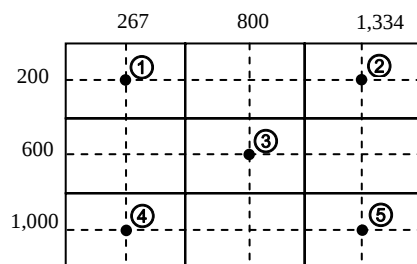
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.13.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

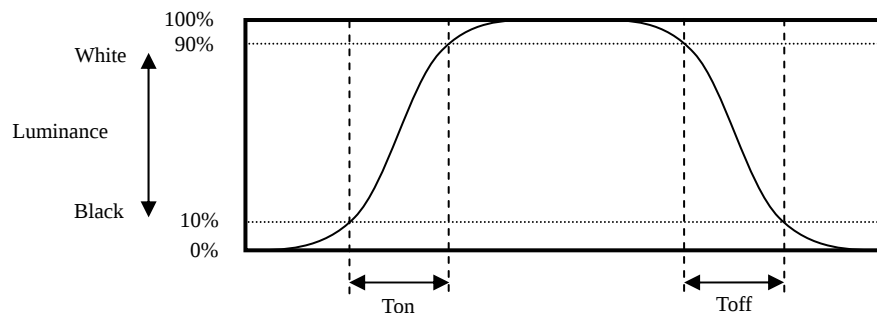
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

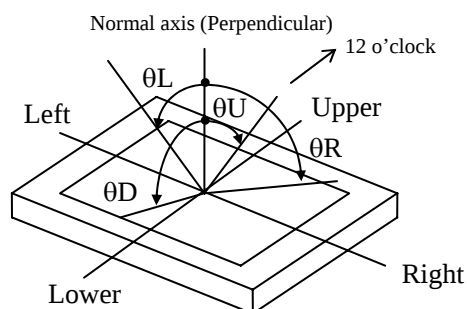


4.13.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.13.5 Definition of viewing angles

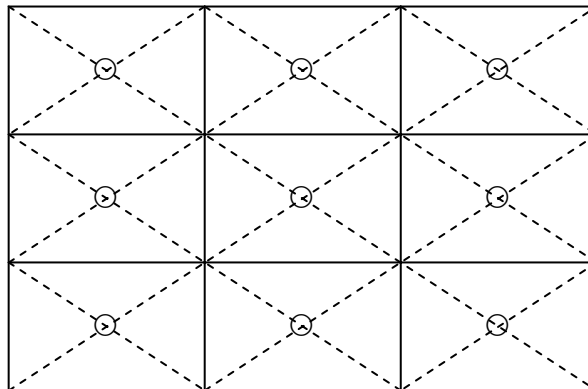


5. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① $60 \pm 2^{\circ}\text{C}$, RH = 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)		① $0 \pm 3^{\circ}\text{C} \dots 1\text{hour}$ $55 \pm 3^{\circ}\text{C} \dots 1\text{hour}$ ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)		① $-20 \pm 3^{\circ}\text{C} \dots 30\text{minutes}$ $60 \pm 3^{\circ}\text{C} \dots 30\text{minutes}$ ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2 , 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω , $\pm 10\text{kV}$ ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	Non-operation	① 15 kPa (Equivalent to altitude 13,600m) ② $-20^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$ ③ $+60^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$	No display malfunctions
	Operation	① 53.3 kPa (Equivalent to altitude 4,850m) ② $0^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$ ③ $+55^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**



This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.



This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.



This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS



*** Do not touch the working backlight and inverter. There is a danger of an electric shock.**



*** Do not touch the working backlight and inverter. There is a danger of burn injury.
* Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N ($\phi 16\text{mm}$ jig))**

6.3 ATTENTIONS



6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.735 N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be $\leq 5.3\text{mm}$.
- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) Bends or twist described above and undue stress to any portion except mounting hole portion may cause display mura.
- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.

- ⑧ Do not push nor pull the interface connectors while the product is working.
- ⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.

6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

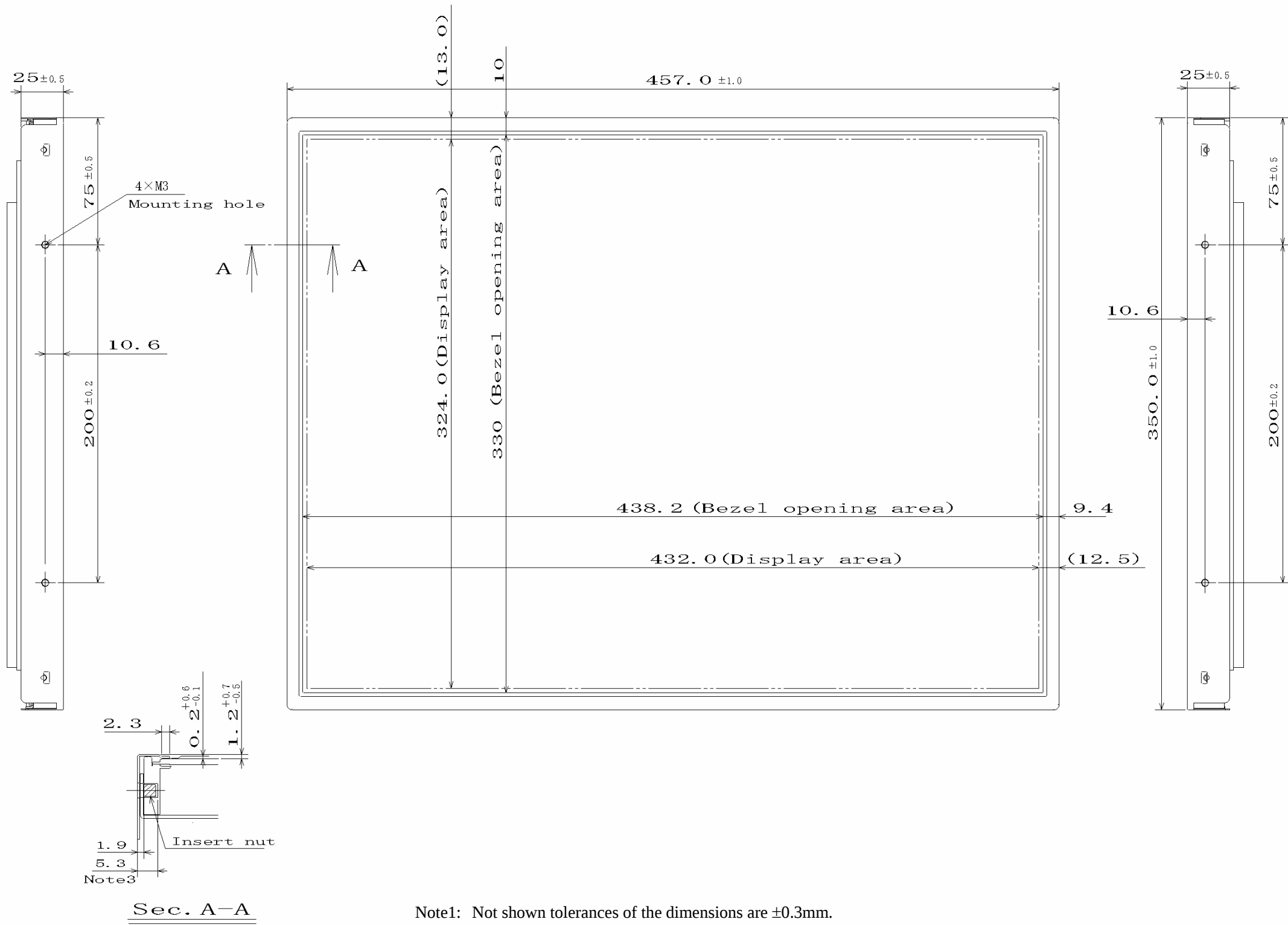
- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

6.3.4 Other

- ① All VDD, VDDB, GND and GNDB terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ See "REPLACEMENT MANUAL FOR INVERTER", when replacing the inverter.
- ④ Pay attention not to insert foreign materials inside of the product, when using tapping screws.
- ⑤ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
- ⑥ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

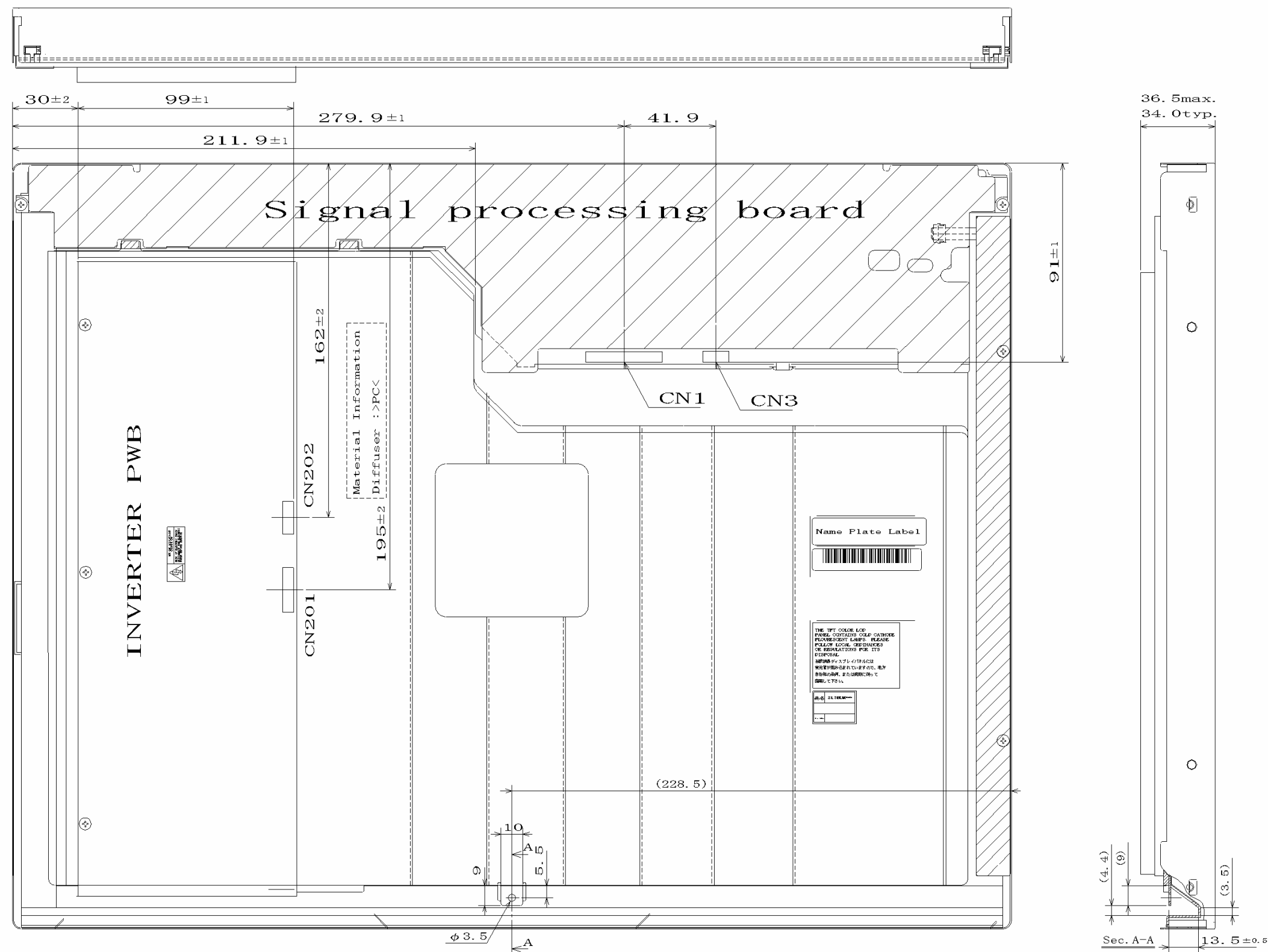
7. OUTLINE DRAWINGS

7.1 FRONT VIEW



Unit: mm

7.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.3mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The values in parentheses are for reference.

Unit: mm