PRELIMINARY

NEC LCD Technologies, Ltd.

TFT COLOR LCD MODULE

NL204153AC21-09

54cm (21.3 Type)
QXGA
LVDS interface (4 ports)

PRELIMINARY DATA SHEET

DOD-PP-0442 (2nd edition)

RoHS Compliant 2002/95/EC

This PRELIMINARY DATA SHEET is updated document from DOD-PP-0281(1).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

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INTRODUCTION

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL204153AC21-09 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Monitor for PC

1.3 FEATURES

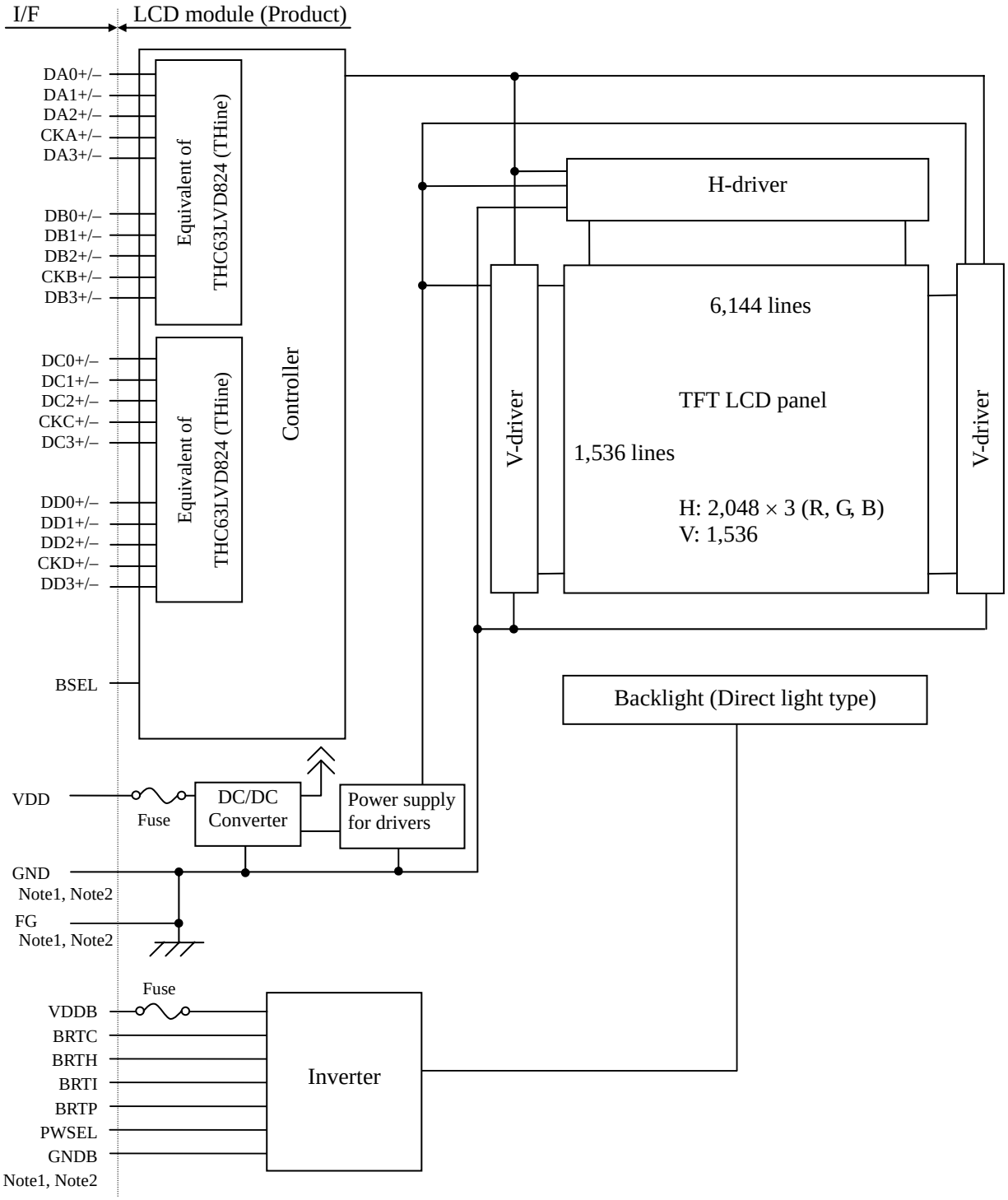
- Ultra-wide viewing angle (Adoption of Ultra-Advanced Super Fine TFT (UA-SFT)) 2
- Wide color gamut 2
- High luminance
- High contrast
- Low reflection
- High resolution QXGA (2,048 × 1,536 pixels, 1 pixel consists of 3 sub-pixels)
- 256 gray scale in each R, G, B sub-pixel (8-bit), 16,777,216 colors 2
- LVDS interface
- Selectable LVDS data input map
- Small foot print
- Incorporated direct light type backlight with an inverter
- Replaceable inverter

2. GENERAL SPECIFICATIONS

Display area	433.152 (H) × 324.864 (V) mm	
Diagonal size of display	54cm (21.3 inches)	
Drive system	a-Si TFT active matrix	
Display color	16,777,216 colors (8-bit)	
Pixel	2,048 (H) × 1,536 (V) pixels (1 pixel consists of 3 sub-pixels (RGB).)	2
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe	
Sub-pixel pitch	0.0705 (H) × 0.2115 (V) mm	
Pixel pitch	0.2115 (H) × 0.2115 (V) mm	
Module size	457.0 (W) × 350.0 (H) × 34.0 (D) mm (typ.)	
Weight	2,700g (typ.)	2
Contrast ratio	750:1 (typ.)	
Viewing angle	*At the contrast ratio ≥ 10:1* • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)	
Designed viewing direction	Viewing angle with optimum grayscale (γ=DICOM): normal axis (perpendicular) Note1	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5400]	
Color gamut	*At LCD panel center* 72 % (typ.) [against NTSC color space]	
Response time	*Ton+Toff (10%←→90%)* 24ms (typ.)	2
Luminance	*At the maximum luminance control* 800cd/m^2 (typ.)	
Signal system	4 ports LVDS interface (THC63LVD824×2pcs, THine Electronics, Inc. or equivalent) [RGB 8-bit signals, Data enable signal (DE), Dot clock (CK)]	
Power supply voltage	LCD panel signal processing board: 12.0V Inverter: 24.0V	
Backlight	Direct light type: 16 cold cathode fluorescent lamps with an inverter (Replaceable part • Inverter: 213PW071)	2
Power consumption	*At checkered flag pattern, the maximum luminance control* 73.2W (typ.)	2

Note1: When the product luminance is 400cd/m^2, the gamma characteristic is designed to γ=DICOM.

3. BLOCK DIAGRAM



2

Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (Inverter ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2 GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 34.0 (typ., D) 37.0 (max. D)	Note1, Note2	mm
Display area	433.152 (H) × 324.864 (V)	Note2	mm
Weight	2,700 (typ.), 2,900 (max.)		g

2

Note1: Excluding warpage of the signal processing board cover and the connection board cover.
Note2: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	-
	Inverter		VDDB	-0.3 to +27.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +2.8	V	VDD= 12.0V
	Inverter	BRTI signal	VBI	-0.3 to +1.5	V	VDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Front surface	TopF	0 to +55	°C	Note2
		Rear surface	TopR	0 to + 60	°C	Note3
Relative humidity Note4			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 70	%	50°C < Ta ≤ 55°C
Absolute humidity Note4			AH	≤ 73 Note5	g/m^3	Ta > 55°C
Operating altitude			-	≤ 4,850	m	0°C≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C≤ Ta ≤ 60°C

2
2
2

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-,BSEL.
Note2: Measured at center of LCD panel surface (including self-heat)
Note3: Measured at center of LCD module's rear shield surface (including self-heat)
Note4: No condensation
Note5: Water amount at Ta= 55°C and RH= 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	500 Note1	900 Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-
Control signal input threshold voltage	High	VIH	Keep this pin open.			-	Note5
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	

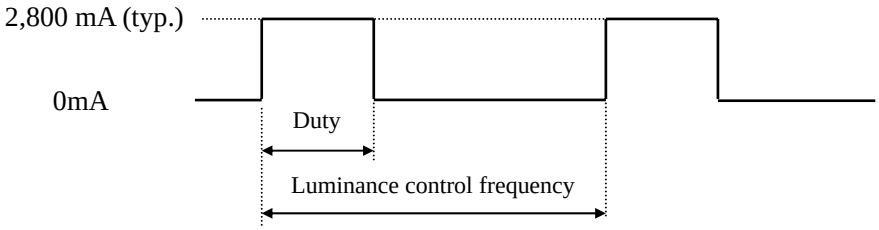
Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS driver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-
Note5: BSEL

4.3.2 Inverter

(Ta= 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage			VDDB	22.8	24.0	25.2	V	-	
Power supply current			IDDB	2,500	2,800	3,100	mA	VDDB= 24.0V, At the maximum luminance control	2
Input voltage for signals	BRTI signal		VBI	0.25	-	1.0	V	-	
	BRTP signal	High	VBPH	2.0	-	5.25	V		
		Low	VBPL	0	-	0.8	V		
	BRTC signal	High	VBCH	2.0	-	5.25	V		
		Low	VBCL	0	-	0.8	V		
	PWSEL signal	High	VPSH	2.0	-	5.25	V		2
		Low	VPSL	0	-	0.8	V		
Input current for signals	BRTI signal		IBI	-200	-	1,000	μA		2
	BRTP signal	High	IBPH	-	-	1,000	μA		2
		Low	IBPL	-600	-	-	μA		
	BRTC signal	High	IBCH	-	-	440	μA		2
		Low	IBCL	-600	-	-	μA		
	PWSEL signal	High	IPSH	-	-	440	μA		2
		Low	IPSL	-600	-	-	μA		

4.3.3 Inverter current wave



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At the maximum luminance control: 100%
At the minimum luminance control: 20%
Luminance control frequency: 255Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of BRTP timing**".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage (See "**4.3.4 Power supply voltage ripple**".) during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

4.3.4 Power supply voltage ripple

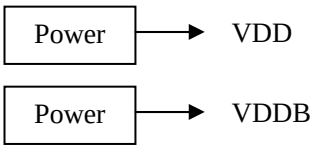
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0V	≤ 100	mVp-p
VDDB	24.0V	≤ 200	mVp-p

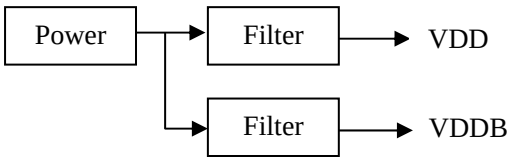
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



4.3.5 Fuse

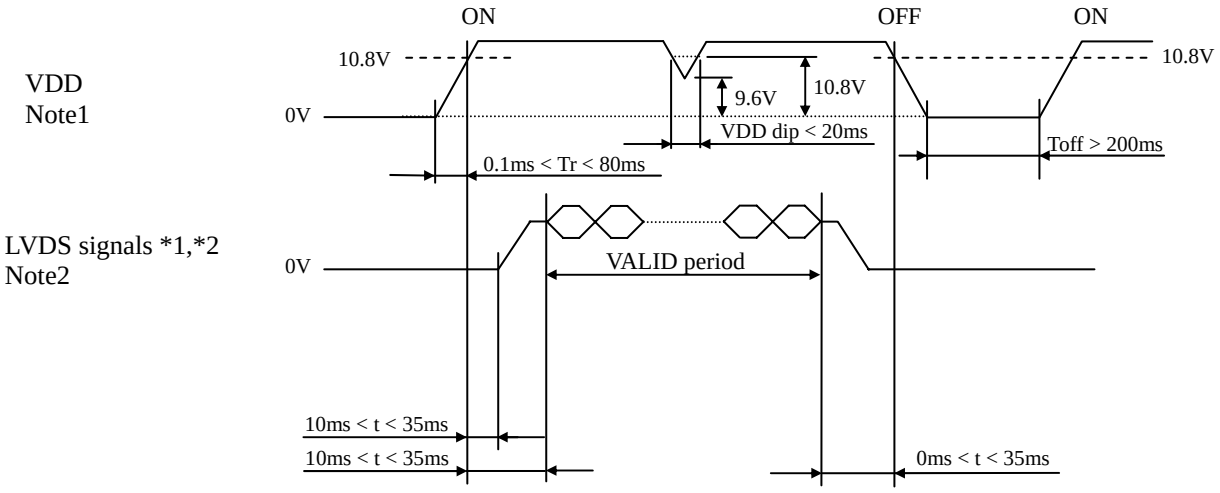
Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	2.0A	4.0A, 5 seconds maximum	Note1
			32V		
VDDB	11CT-6.3A	SOC	6.3A	10A, 5 seconds maximum	
			72V		

2

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-

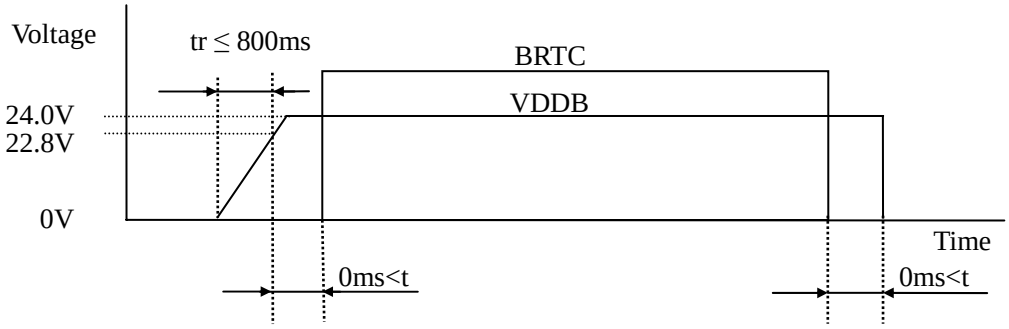
*2: LVDS signals should be measured at the terminal of 100 Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: LVDS signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged. 2
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note3: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display. 2

4.4.2 Inverter



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Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If tr is more than 800ms, the backlight will be turned off by a protection circuit for inverter.

Note3: When VDDB is ON and BRTC is high, voltage to BRTI, BRTP and PWSEL terminals should be applied.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

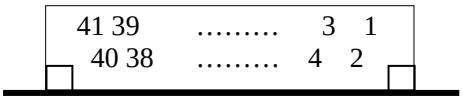
4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-WE41P-HFE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W41S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	RSVD1	Reserved	Connect to signal ground.
2	N.C.	-	Keep this pin Open.
3	N.C.	-	
4	N.C.	-	
5	N.C.	-	
6	N.C.	-	
7	N.C.	-	
8	N.C.	-	
9	BSEL	Selection of LVDS data input map (Pull-up 25kΩ)	See "**4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER**". BSEL: Open → A; Low → C
10	RSVD2	Reserved	Keep this pin Open.
11	GND	Signal ground	Note1
12	DB3+	Pixel data B3	LVDS differential data input Note2
13	DB3-		
14	GND	Signal ground	Note1
15	CKB+	Pixel clock B	LVDS differential clock input Note2
16	CKB-		
17	GND	Signal ground	Note1
18	DB2+	Pixel data B2	LVDS differential data input Note2
19	DB2-		
20	GND	Signal ground	Note1
21	DB1+	Pixel data B1	LVDS differential data input Note2
22	DB1-		
23	GND	Signal ground	Note1
24	DB0+	Pixel data B0	LVDS differential data input Note2
25	DB0-		
26	GND	Signal ground	Note1
27	DA3+	Pixel data A3	LVDS differential data input Note2
28	DA3-		
29	GND	Signal ground	Note1
30	CKA+	Pixel clock A	LVDS differential clock input Note2
31	CKA-		
32	GND	Signal ground	Note1
33	DA2+	Pixel data A2	LVDS differential data input Note2
34	DA2-		
35	GND	Signal ground	Note1
36	DA1+	Pixel data A1	LVDS differential data input Note2
37	DA1-		
38	GND	Signal ground	Note1
39	DA0+	Pixel data A0	LVDS differential data input Note2
40	DA0-		
41	GND	Signal ground	Note1

Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN1: View from insert direction

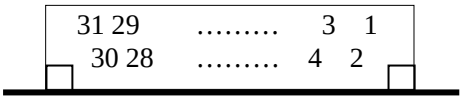


CN2 socket (LCD module side): FI-WE31P-HFE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W31S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Signal ground	Note1
2	DD3+	Pixel data D3	LVDS differential data input Note2
3	DD3-		
4	GND	Signal ground	Note1
5	CKD+	Pixel clock D	LVDS differential clock input Note2
6	CKD-		
7	GND	Signal ground	Note1
8	DD2+	Pixel data D2	LVDS differential data input Note2
9	DD2-		
10	GND	Signal ground	Note1
11	DD1+	Pixel data D1	LVDS differential data input Note2
12	DD1-		
13	GND	Signal ground	Note1
14	DD0+	Pixel data D0	LVDS differential data input Note2
15	DD0-		
16	GND	Signal ground	Note1
17	DC3+	Pixel data C3	LVDS differential data input Note2
18	DC3-		
19	GND	Signal ground	Note1
20	CKC+	Pixel clock C	LVDS differential clock input Note2
21	CKC-		
22	GND	Signal ground	Note1
23	DC2+	Pixel data C2	LVDS differential data input Note2
24	DC2-		
25	GND	Signal ground	Note1
26	DC1+	Pixel data C1	LVDS differential data input Note2
27	DC1-		
28	GND	Signal ground	Note1
29	DC0+	Pixel data C0	LVDS differential data input Note2
30	DC0-		
31	GND	Signal ground	Note1

Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN2: View from insert direction



CN3 socket (LCD module side): IL-Z-8PL-SMTY (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-8S-S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	Note1
2	VDD		
3	VDD		
4	VDD		
5	GND	Signal ground	Note1
6	GND		
7	GND		
8	GND		

Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 Inverter

CN201 socket (LCD module side): DF3Z-10P-2H (2∗) (HIROSE ELECTRIC Co,.Ltd.)
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co,.Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

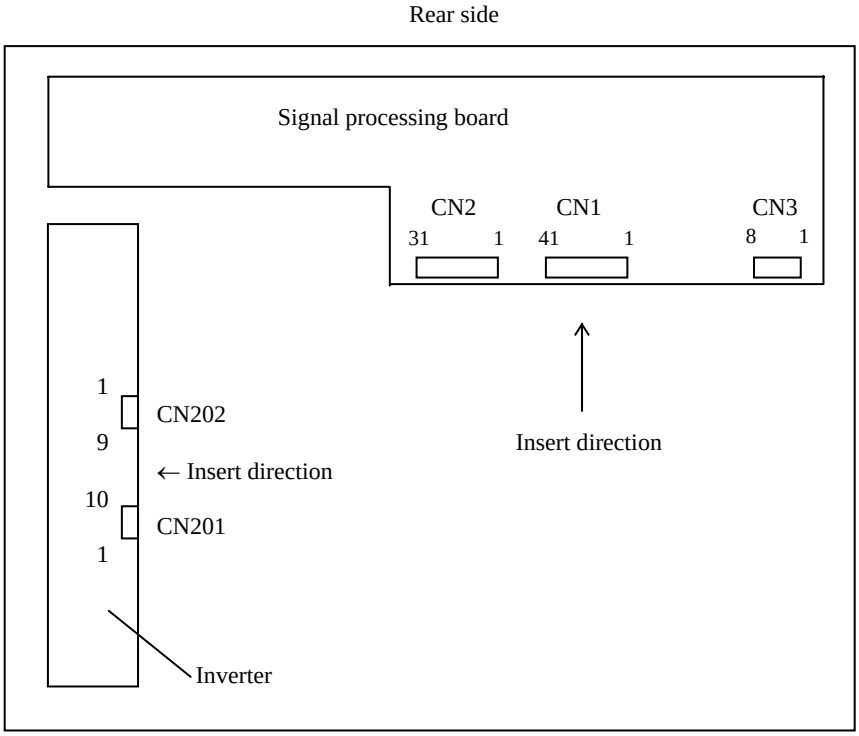
Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	Note2, Note3
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	Inverter ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: See "**4.6.1 LUMINANCE CONTROL** ".
Note3: When VDDB is ON and BRTC is high, voltage to BRTI, BRTP and PWSEL terminals should be applied.

4.5.3 Positions of socket

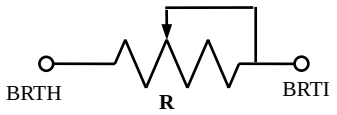


4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL terminal</th><th>BRTP terminal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment

The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.
The resistor (R) must be connected between BRTH-BRTI terminals.
 

• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>1.5kΩNote4</td><td>20% (Min. Luminance)</td></tr><tr><td>10kΩ</td><td>100% (Max. Luminance)</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1
Note5</td><td>• Adjustment

Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.
Luminance is the maximum when BRTI terminal is Open.

• Luminance ratio Note3
<table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0.2V Note4</td><td>20% (Min. Luminance)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table></td></tr>
<tr><td>Pulse width modulation

Note1
Note2
Note6</td><td>• Adjustment

Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.

• Luminance ratio Note3
<table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>0.2 Note4</td><td>20% (Min. Luminance)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table></td><td>Low</td><td>BRTP signal</td></tr>
</table>

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.
Use PWM method, if interference noises appear on the display image!

Note2: The inverter will stop working, if the Low period of BRTP signal is more than 500ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The inverter will start to work when power is supplied again. 2

Note3: These data are the target values.

Note4: Do not set the variable resistor, BRTI voltage and Pulse width modulation in less than 1.5kΩ or less than 0.2V or less than 0.2(Duty ratio). Otherwise flicker or display mura may cause, or the lamp may not be turned on. 2

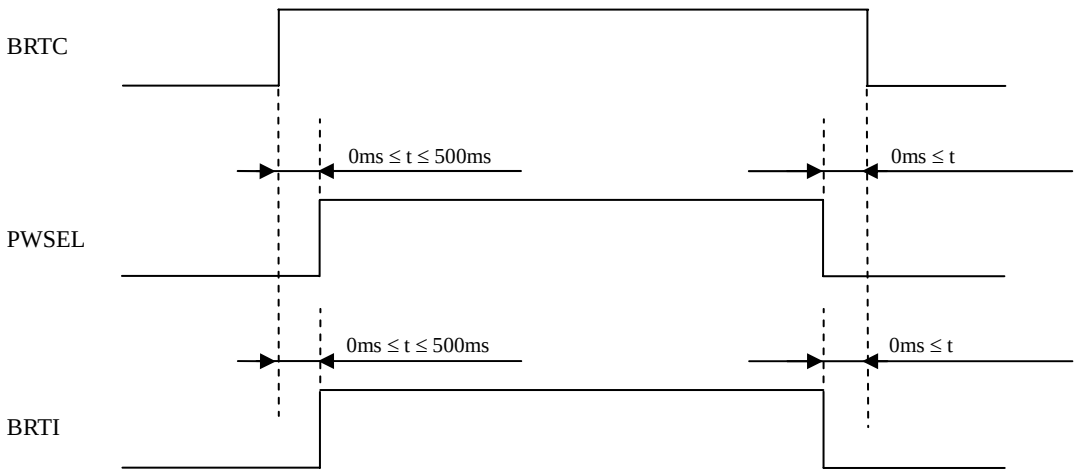
Note5: See "**4.6.2 Detail of BRTI timing**".

Note6: See "**4.6.3 Detail of BRTP timing**". 2

4.6.2 Detail of BRTI timing

(1) Timing diagrams

2

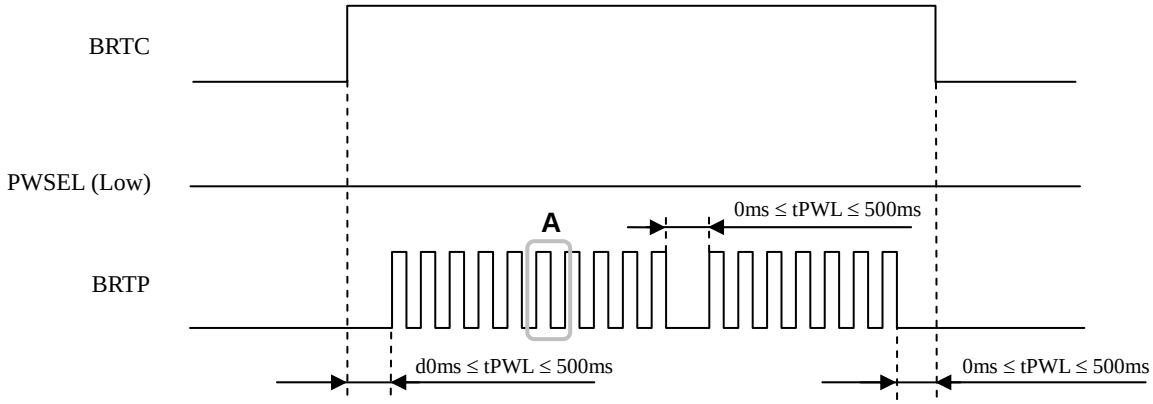


Note1: When VDDB is ON and BRTC is high, voltage to BRTI, BRTP and PWSEL terminals should be applied.

4.6.3 Detail of BRTP timing

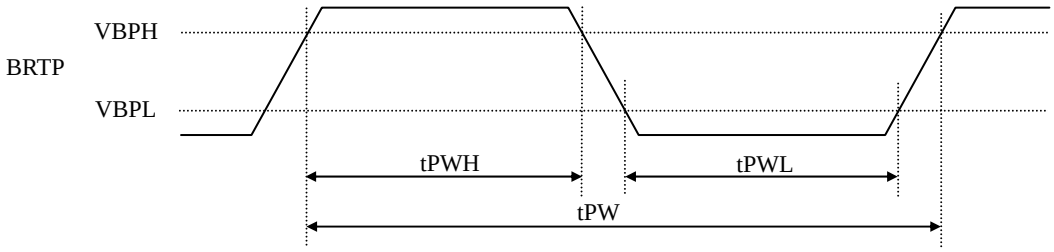
(1) Timing diagrams

- Outline chart



2

- Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	185	-	325	Hz	Note1, Note2
Duty ratio	DL	0.2	-	1.0	-	Note1, Note3
Low period	tPWL	0	-	500	ms	Note4

2

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW}, \quad DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.

Luminance control frequency= 1/tv × (n+0.25) [or (n+0.75)]
n = 1, 2, 3 · · · · · ·
tv: Vertical cycle (See "**4.9.1 Timing characteristics**".)

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "**4.6.1 Luminance control methods**".

Note4: If tPWL is more than 500ms, the backlight will be turned off by a protection circuit for inverter. The inverter will start to work when power is supplied again.

2

Note5: When VDDB is ON and BRTC is high, voltage to BRTI, BRTP and PWSEL terminals should be applied.

4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER

LVDS data input map is selectable by BSEL terminal.

	Bit mapping			Transmitter Pin Assignment					CN1	
	BSEL Note1			Single type LVDS Tx	Dual type LVDS TX		Output Connector			
	[H] Mode A		[L] Mode C		THine THC63LVD823	NS DS90C387			Pin No.	Signal name
Pixel data A	RA2		RA0	TA0	R12	R10				
	RA3		RA1	TA1	R13	R11		Note2		
	RA4		RA2	TA2	R14	R12	ATA-	→	40	DA0-
	RA5		RA3	TA3	R15	R13	ATA+	→	39	DA0+
	RA6		RA4	TA4	R16	R14				
	RA7		RA5	TA5	R17	R15				
	GA2		GA0	TA6	G12	G10				
	GA3		GA1	TB0	G13	G11				
	GA4		GA2	TB1	G14	G12				
	GA5		GA3	TB2	G15	G13	ATB-	→	37	DA1-
	GA6		GA4	TB3	G16	G14	ATB+	→	36	DA1+
	GA7		GA5	TB4	G17	G15				
	BA2		BA0	TB5	B12	B10				
	BA3		BA1	TB6	B13	B11				
	BA4		BA2	TC0	B14	B12				
	BA5		BA3	TC1	B15	B13				
	BA6		BA4	TC2	B16	B14	ATC-	→	34	DA2-
	BA7		BA5	TC3	B17	B15	ATC+	→	33	DA2+
	Hsync		Hsync	TC4	HSYNC	HSYNC				
	Vsync		Vsync	TC5	VSYNC	VSYNC				
	DE		DE	TC6	DE	DE				
	RA0		RA6	TD0	R10	R16				
	RA1		RA7	TD1	R11	R17				
	GA0		GA6	TD2	G10	G16	ATD-	→	28	DA3-
	GA1		GA7	TD3	G11	G17	ATD+	→	27	DA3+
	BA0		BA6	TD4	B10	B16				
	BA1		BA7	TD5	B11	B17				
	N.C.		N.C.	TD6	-	-				
	CLK		CLK	CLK	CLK	CLK	ATCLK-	→	31	CKA-
							ATCLK+	→	30	CKA+
Pixel data B	RB2		RB0	TA0	R22	R20				
	RB3		RB1	TA1	R23	R21				
	RB4		RB2	TA2	R24	R22	BTA-	→	25	DB0-
	RB5		RB3	TA3	R25	R23	BTA+	→	24	DB0+
	RB6		RB4	TA4	R26	R24				
	RB7		RB5	TA5	R27	R25				
	GB2		GB0	TA6	G22	G20				
	GB3		GB1	TB0	G23	G21				
	GB4		GB2	TB1	G24	G22				
	GB5		GB3	TB2	G25	G23	BTB-	→	22	DB1-
	GB6		GB4	TB3	G26	G24	BTB+	→	21	DB1+
	GB7		GB5	TB4	G27	G25				
	BB2		BB0	TB5	B22	B20				
	BB3		BB1	TB6	B23	B21				
	BB4		BB2	TC0	B24	B22				
	BB5		BB3	TC1	B25	B23				
	BB6		BB4	TC2	B26	B24	BTC-	→	19	DB2-
	BB7		BB5	TC3	B27	B25	BTC+	→	18	DB2+
	Hsync		Hsync	TC4	HSYNC	HSYNC				
	Vsync		Vsync	TC5	VSYNC	VSYNC				
	DE		DE	TC6	DE	DE				
	RB0		RB6	TD0	R20	R26				
	RB1		RB7	TD1	R21	R27				
	GB0		GB6	TD2	G20	G26	BTD-	→	13	DB3-
	GB1		GB7	TD3	G21	G27	BTD+	→	12	DB3+
	BB0		BB6	TD4	B20	B26				
	BB1		BB7	TD5	B21	B27				
	N.C.		N.C.	TD6	-	-				
	CLK		CLK	CLK	CLK	CLK	BTCLK-	→	16	CKB-
							BTCLK+	→	15	CKB+

	BSEL Note1 [H] Mode A	[L] Mode C	Single type LVDS Tx	Dual type LVDS TX THine THC63LVD823	Dual type LVDS TX NS DS90C387	Output Connector		CN2 Pin No.	CN2 Signal name
Pixel data C	RC2	RC0	TA0	R12	R10				
	RC3	RC1	TA1	R13	R11		Note2		
	RC4	RC2	TA2	R14	R12	CTA-	→	30	DC0-
	RC5	RC3	TA3	R15	R13	CTA+	→	29	DC0+
	RC6	RC4	TA4	R16	R14				
	RC7	RC5	TA5	R17	R15				
	GC2	GC0	TA6	G12	G10				
	GC3	GC1	TB0	G13	G11				
	GC4	GC2	TB1	G14	G12				
	GC5	GC3	TB2	G15	G13	CTB-	→	27	DC1-
	GC6	GC4	TB3	G16	G14	CTB+	→	26	DC1+
	GC7	GC5	TB4	G17	G15				
	BC2	BC0	TB5	B12	B10				
	BC3	BC1	TB6	B13	B11				
	BC4	BC2	TC0	B14	B12				
	BC5	BC3	TC1	B15	B13				
	BC6	BC4	TC2	B16	B14	CTC-	→	24	DC2-
	BC7	BC5	TC3	B17	B15	CTC+	→	23	DC2+
	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	TC6	DE	DE				
	RC0	RC6	TD0	R10	R16				
	RC1	RC7	TD1	R11	R17				
	GC0	GC6	TD2	G10	G16	CTD-	→	18	DC3-
	GC1	GC7	TD3	G11	G17	CTD+	→	17	DC3+
	BC0	BC6	TD4	B10	B16				
	BC1	BC7	TD5	B11	B17				
	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CTCLK-	→	21	CKC-
						CTCLK+	→	20	CKC+
Pixel data D	RD2	RD0	TA0	R22	R20				
	RD3	RD1	TA1	R23	R21				
	RD4	RD2	TA2	R24	R22	DTA-	→	15	DD0-
	RD5	RD3	TA3	R25	R23	DTA+	→	14	DD0+
	RD6	RD4	TA4	R26	R24				
	RD7	RD5	TA5	R27	R25				
	GD2	GD0	TA6	G22	G20				
	GD3	GD1	TB0	G23	G21				
	GD4	GD2	TB1	G24	G22				
	GD5	GD3	TB2	G25	G23	DTB-	→	12	DD1-
	GD6	GD4	TB3	G26	G24	DTB+	→	11	DD1+
	GD7	GD5	TB4	G27	G25				
	BD2	BD0	TB5	B22	B20				
	BD3	BD1	TB6	B23	B21				
	BD4	BD2	TC0	B24	B22				
	BD5	BD3	TC1	B25	B23				
	BD6	BD4	TC2	B26	B24	DTC-	→	9	DD2-
	BD7	BD5	TC3	B27	B25	DTC+	→	8	DD2+
	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	TC6	DE	DE				
	RD0	RD6	TD0	R20	R26				
	RD1	RD7	TD1	R21	R27				
	GD0	GD6	TD2	G20	G26	DTD-	→	3	DD3-
	GD1	GD7	TD3	G21	G27	DTD+	→	2	DD3+
	BD0	BD6	TD4	B20	B26				
	BD1	BD7	TD5	B21	B27				
	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	DTCLK-	→	6	CKD-
						DTCLK+	→	5	CKD+

Note1: High must be Open.

Note2: Do not change the setting of BSEL during VDD ON period.

Note3: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

2

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 gray scale in each R, G, B sub-pixel. Also the relation between display colors and input data signals is as the following table. 2

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
		RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
		RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

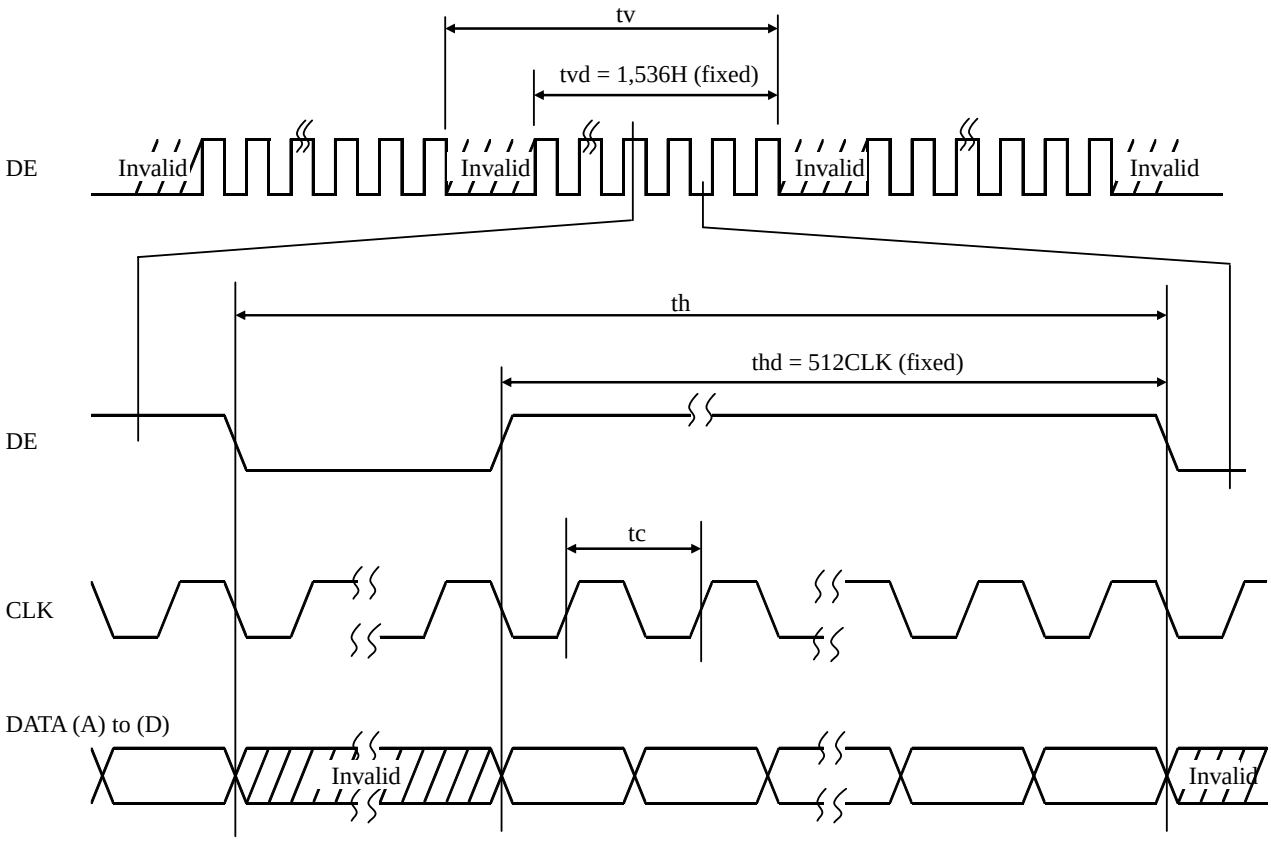
4.9 INPUT SIGNAL TIMINGS

4.9.1 Timing characteristics

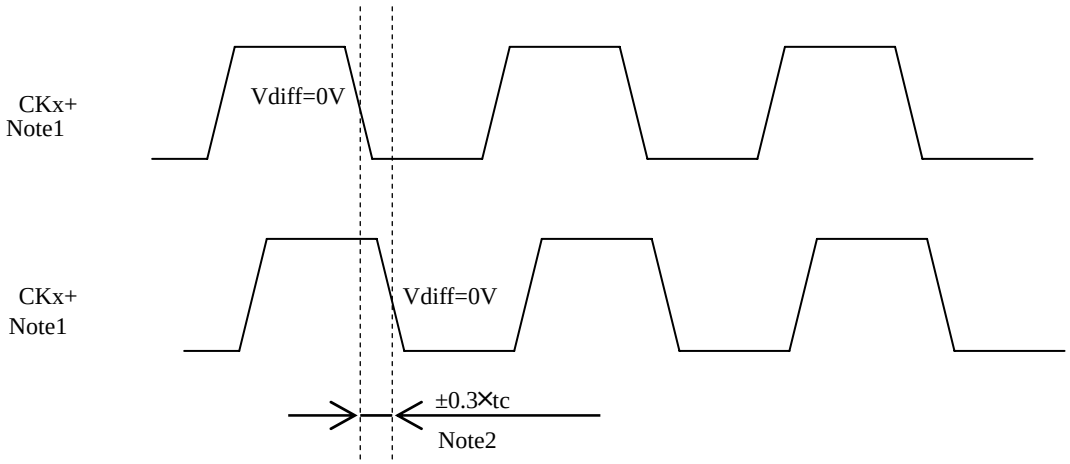
Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/ tc	60.0	65.0	66.0	MHz	15.38ns (typ.)
	Duty		-	See the data sheet of LVDS transmitter.			-	-
	Rise time, Fall time		-				ns	-
DE	Horizontal	Cycle	th	10.34	10.34	10.77	µs	96.72kHz (typ.) Note1
				640	672	700	CLK	
		Display period	thd	512			CLK	-
	Vertical	Cycle	tv	15.47	16.667	17.9	ms	60.0Hz (yp.)
				1,547	1,612	1,628	H	
		Display period	tvd	1,536			H	-
	CLK-DE	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-
DATA (A) to (D)	CLK-DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-

Note1: During operation, fluctuation of horizontal cycle should be within ±1 CLK. 2

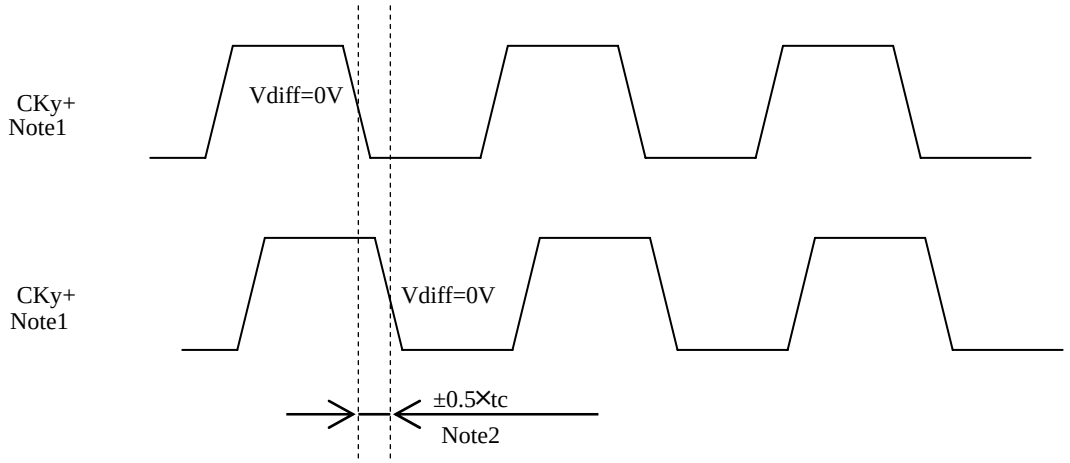
4.9.2 Input signal timing chart



2

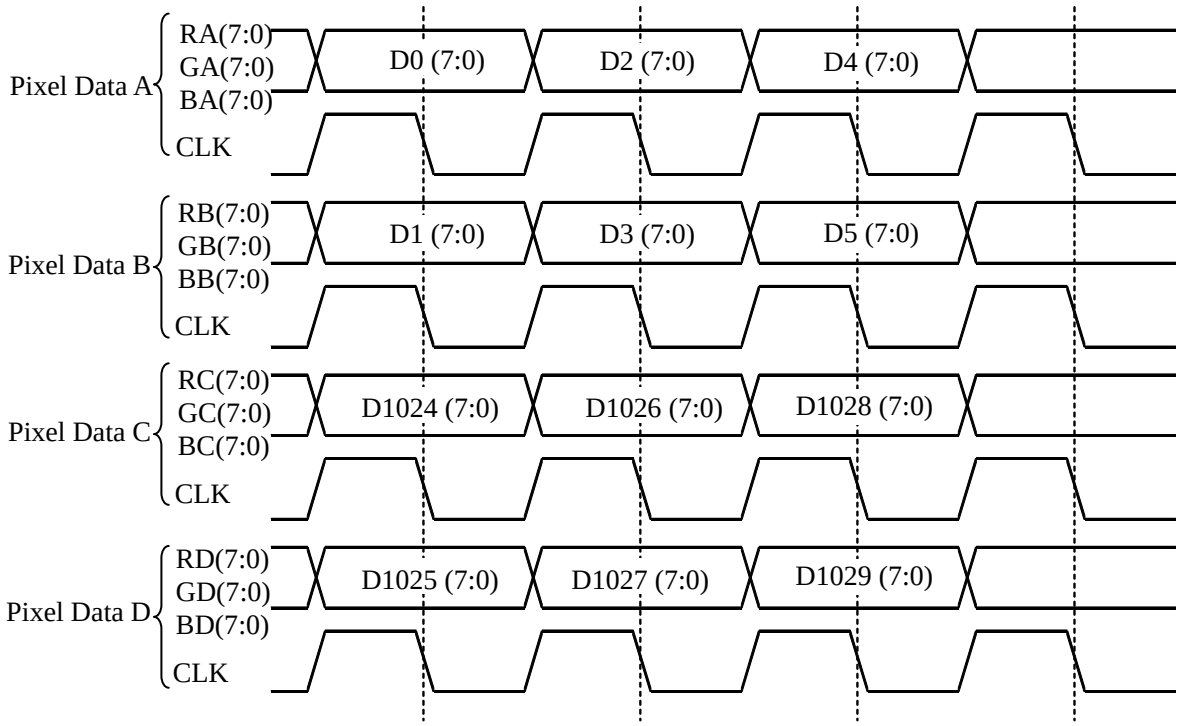


Note1: Combination: x=A,B and x=C,B
Note2: CKA+ - CKB+ ≤+ 0.3 tc, CKC+ - CKD+ ≤+ 0.3 tc

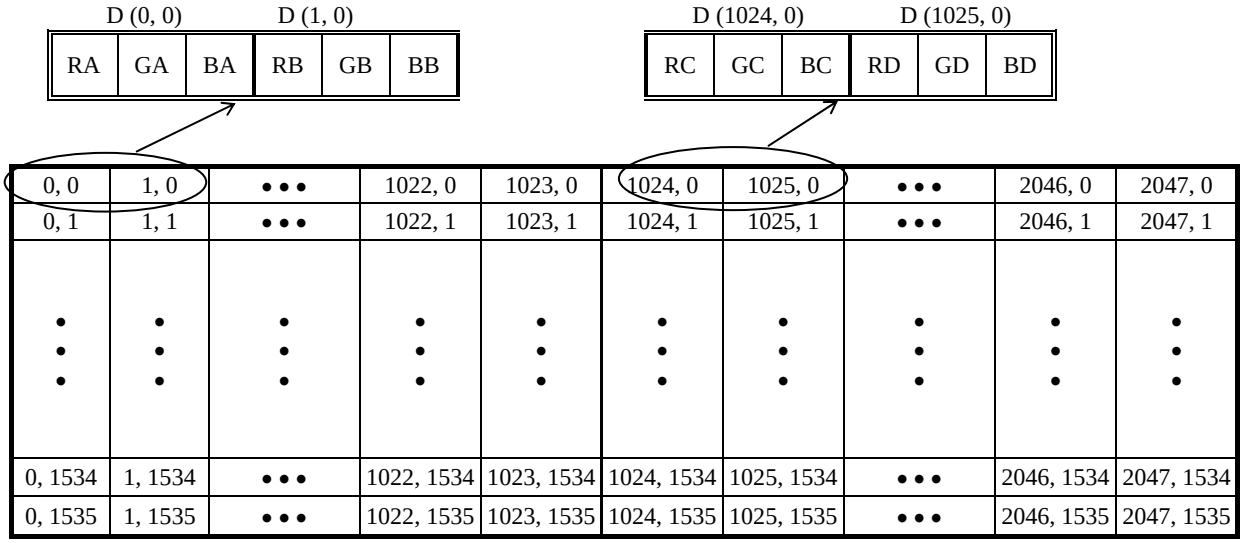


Note1: Combination: y=A,C and y=A,D and y=B,C and y=B,D
Note2: CKA+ - CKC+ ≤+ 0.5 tc, CKA+ - CKD+ ≤+ 0.5 tc
CKB+ - CKC+ ≤+ 0.5 tc, CKB+ - CKD+ ≤+ 0.5 tc

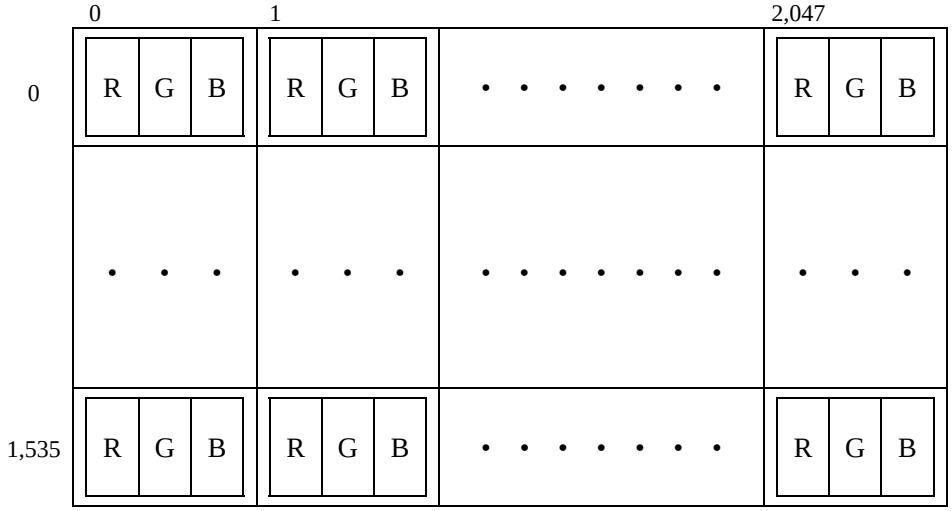
4.10 LVDS DATA TARANSMISSION METHOD



4.11 DISPLAY POSITIONS



4.12 PIXEL ARRANGNMENT



4.13 OPTICS

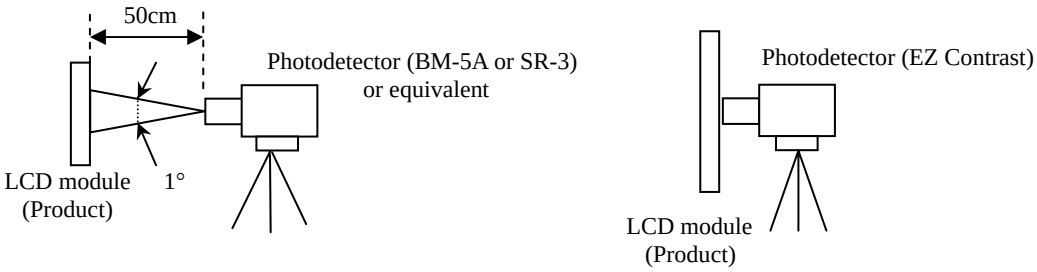
4.13.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	650	800	-	cd/m^2	BM-5A or SR-3	Note3	2
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	600	750	-	-	BM-5A or SR-3	Note3 Note5	
Luminance uniformity		0/255 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU_0	50	-	-	%	BM-5A or SR-3	Note4 Note6	2
		26/255 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU_{26}	65	-	-				
		128/255 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU_{128}	70	-	-				
		204/255 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU_{204}	70	-	-				
		255/255 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU_{255}	75	-	-				
Chromaticity	White	**x** coordinate	Wx	0.293	0.313	0.333	-	SR-3	Note3 Note7	
		y coordinate	Wy	0.309	0.329	0.349	-			
	Red	**x** coordinate	Rx	-	0.650	-	-			2
		y coordinate	Ry	-	0.330	-	-			
	Green	**x** coordinate	Gx	-	0.290	-	-			2
		y coordinate	Gy	-	0.610	-	-			
	Blue	**x** coordinate	Bx	-	0.150	-	-			2
		y coordinate	By	-	0.060	-	-			
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	65	72	-	%	SR-3	Note3	2
Response time		Black to White	Ton	-	14	20	ms	BM-5A	Note3 Note8	2
		White to Black	Toff	-	10	15	ms			
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	70	85	-	°	EZ Contrast	Note3 Note9	
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	70	85	-	°			
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	70	85	-	°			
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	70	85	-	°			

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
Ta= 25°C, VDD= 12.0V, VDDB= 24.0V, Display mode: QXGA,
Horizontal cycle= 1/96.72 kHz, Vertical cycle= 1/60.0 Hz

Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: Product surface temperature at the maximum luminance control: TopF = 40°C 2
Note4: Product surface temperature at 400cd/m^2 luminance control: TopF = 33°C 2
Note5: See "**4.13.2 Definition of contrast ratio**".
Note6: See "**4.13.3 Definition of luminance uniformity**".
Note7: These coordinates are found on CIE 1931 chromaticity diagram.
Note8: See "**4.13.4 Definition of response times**".
Note9: See "**4.13.5 Definition of viewing angles**".

4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.13.3 Definition of luminance uniformity

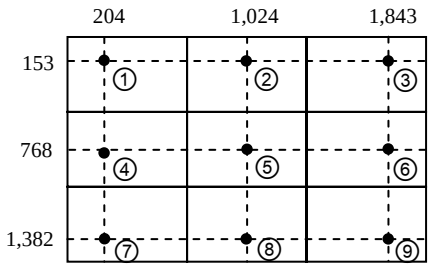
2

The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity (LUxx)} = \frac{\text{Minimum luminance from ① to ⑨}}{\text{Maximum luminance from ① to ⑨}}$$

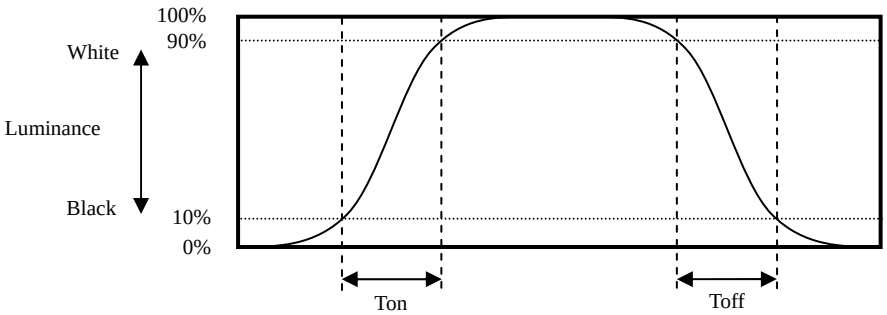
xx: 0, 26, 128, 204, 255 gray scale.

The luminance is measured at near the 9 points shown below.

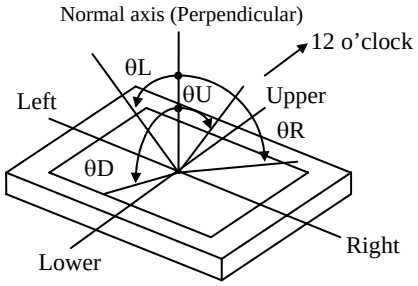


4.13.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



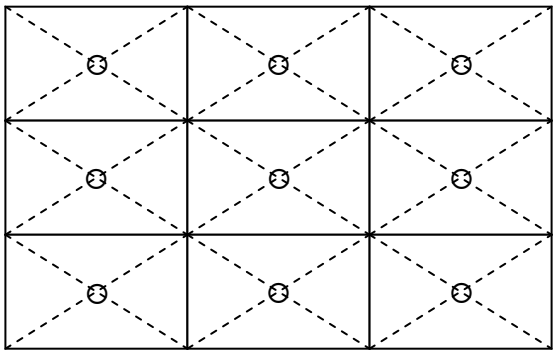
4.13.5 Definition of viewing angles



5. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH= 60%, 240hours ② Display data is white. Note2	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white. Note2	
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2, 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note3 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval Note2	
Low pressure	Non-operation	① 15kPa (Equivalent to altitude 13,600m) ② -20°C±3°C…24 hours ③ +60°C±3°C…24 hours	No display malfunctions
	Operation	① 53.3kPa (Equivalent to altitude 4,850m) ② 0°C±3°C…24 hours ③ +55°C±3°C…24 hours Note2	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.
Note2: Luminance: 400cd/m^2 at luminance control.
Note3: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

⚠	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
⚡	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
✋	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

⚡

- **Do not touch the working backlight. There is a danger of an electric shock.**

✋

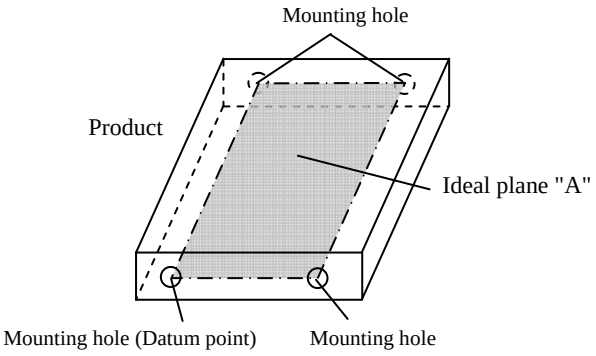
- **Do not touch the working backlight. There is a danger of burn injury.**
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N (ϕ16mm jig))**

6.3 ATTENTIONS ⚠

6.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed 0.735N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 4.7mm.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
⑧ Do not push nor pull the interface connectors while the product is working.
⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal for the worst, please wash it out with soap.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed depending on input signal timings.
⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.
⑧ After the product is stored under condition of low temperature or dark place for a long time, the cold cathode fluorescent lamp may not be turned on under the same condition because of the general characteristic of cold cathode fluorescent lamp. In addition, when Luminance control ratio is low in pulse width modulation method inverter, the lamp may not be turned on. In this case, power should be supplied again.

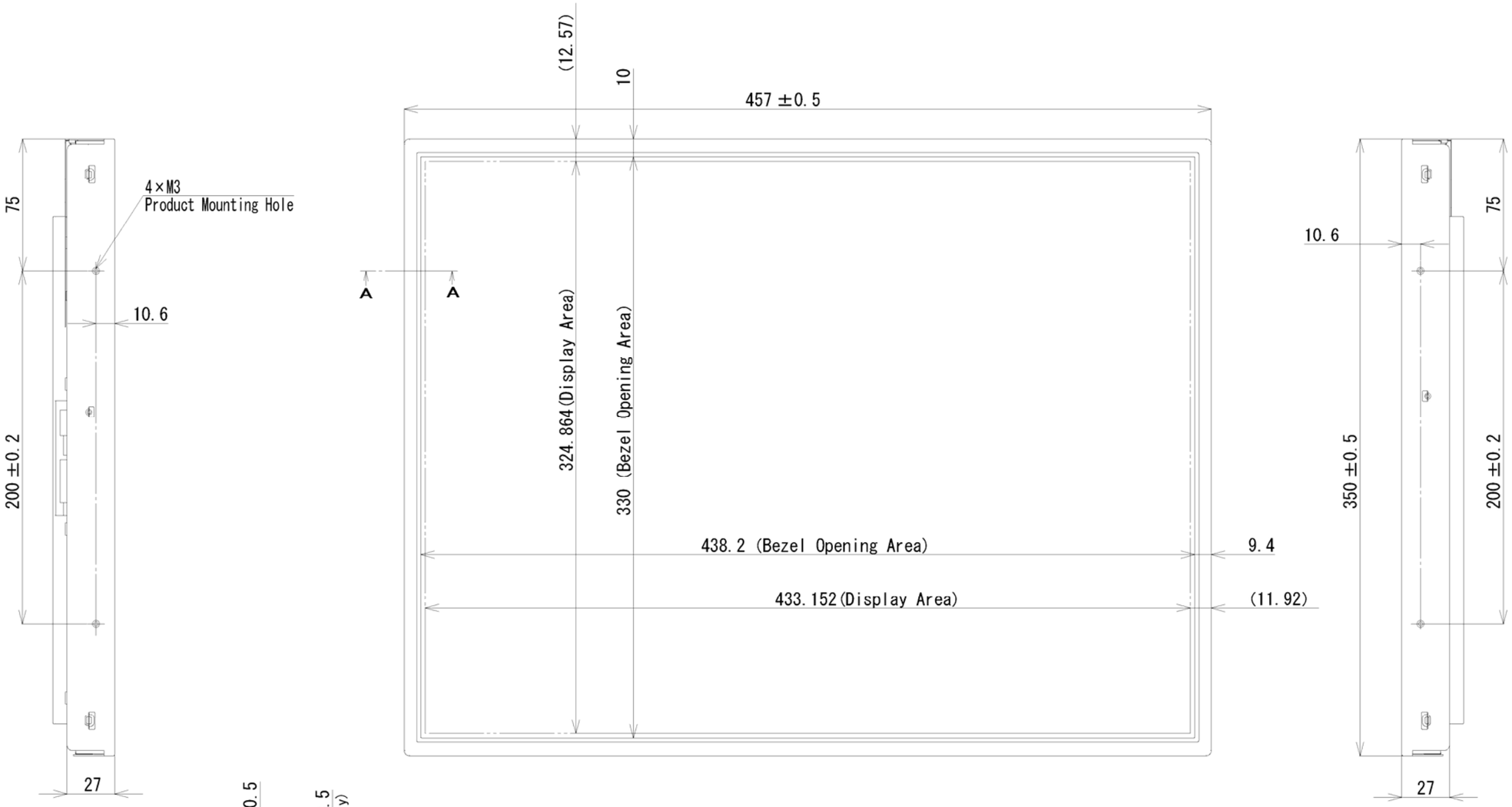
2

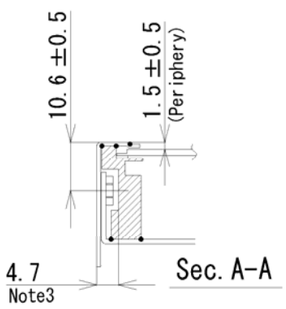
6.3.4 Other

① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ See "REPLACEMENT MANUAL FOR INVERTER", when replacing backlight lamps.
④ Pay attention not to insert foreign materials inside of the product, when using tapping screws.
⑤ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
⑥ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

7. OUTLINE DRAWINGS

7.1 FRONT VIEW

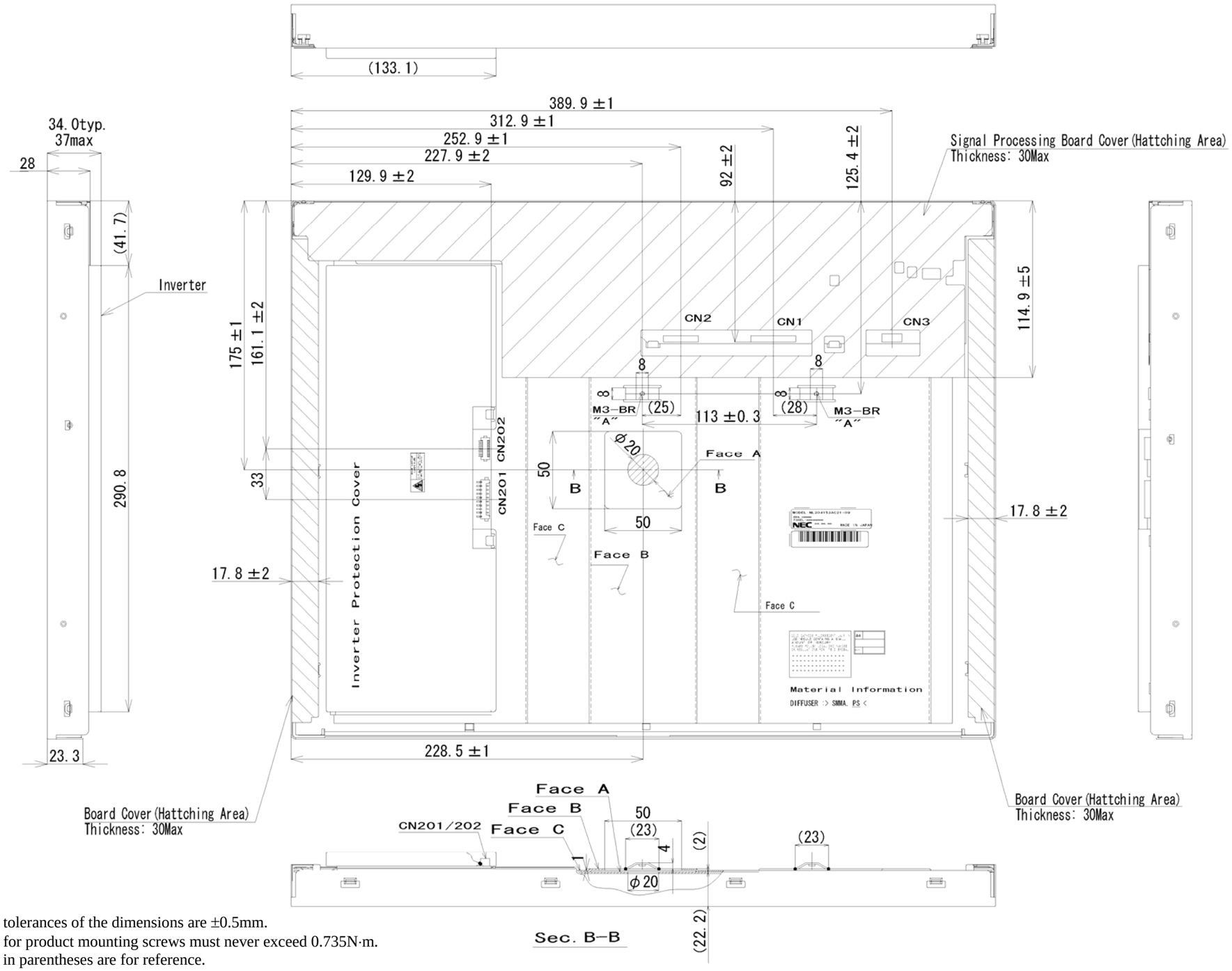




Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 4.7mm.
Note4: The values in parentheses are for reference.

Unit: mm

7.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The values in parentheses are for reference.
Note4: The torque for the holes "A" must never exceed 0.44N·m.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-0281	June 29, 2007	**Revision contents** New issue **Signature of writer** *Approved by* T. OGAWA *Checked by* _____ *Prepared by* T. OGAWA
2nd edition	DOD-PP-0442	Jan. 23, 2007	**Revision contents** P4 Future •Super-Advanced Super Fine TFT (SA-SFT) → Ultra-Advanced Super Fine TFT (UA-SFT) (correction) •Wide color gamut (addition) •256 gray scale in each R, G, B sub-pixel (8-bit), 16,777,216 colors (addition) P5 General spcifications •Pixel: 1 pixel consists of 3 sub-pixels (LCR) → 1 pixel consists of 3 sub-pixels (RGB) (correction) •Weight: 3,000 g (typ.) → 2,700 g (typ.) •Respnse time: 27 ms (typ.) → 24 ms (typ.) •Backlight - Replacealbe part: TBD → 213PW071 •Power consumption: 80.4W → 73.2W P6 Block diagram •CS, SCLK, SDAT, BSEL0, BSEL1 → BSEL P7 Mechanical specifications •Weight: 3,000 g (typ.), 3,200 g (max.) → 2,700 g (typ.), 2,900 g (max.) •Note1: CS, SCLK, SDAT, BSEL0, BSEL1 → BSEL P7 Absolute maximum ratings •Relative humidity: ≤ 95, Ta ≤ 40°C, ≤ 85, 40°C < Ta ≤ 50°C (addition) •Relative humidity - ≤ 70: Ta ≤ 55°C → 50°C < Ta ≤ 55°C (change) P8 Electrical characteristics - LCD panel signal processing board •Power supply current: 700 mA (typ.), 1,250 mA (max.) → 500 mA (typ.), 900 mA (typ.) P9 Electrical characteristics - Inverter •Power supply current: - (min.), 3,000 mA (typ.), TBD mA (max.) → 2,500 mA (min.), 2,800 mA (typ.), 3,100 mA (max.) •VPSLH,VPSLL → VPSH,VPSL (change) •Input current for signals - BRTI signal: TBD μA (min.) TBD μA (max.) → -200 μA (min.), 1,000 μA (max.) •Input current for signals - BRTP signal: TBD μA (min.) TBD μA (max.) → -600 μA (min.), 1,000 μA (max.) •Input current for signals - BRTC signal: TBD μA (min.) TBD μA (max.) → -600 μA (min.), 440 μA (max.) •Input current for signals - PWSEL signal: TBD μA (min.) TBD μA (max.) → -600 μA (min.), 440 μA (max.) (change) P9 Inverter current wave •2,700mA (typ.) → 2,800mA (typ.)

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
2nd edition	DOD-PP-0422	Jan 23, 2008	**Revision contents** P10 Fuse •VDDB (specified) P11 LCD panel signal processing board •Note2: and, CS, SDLK, DS (elimination) •Note3 (addition) P11 Inverter (specified) P14 Inverter •CN202: Note3 (addition) P16 Luminance control methods •BRTI Voltage: 0.25V → 0.2V (change) •Note2: more than 50ms → more than 500ms (addition) •Note4: Duty ratio → Pulse width modulation, 0.25V → 0.2V, 20% → 0.2 (Duty ratio) •Note5 (addition) P17 Detail of BRTI timing (addition) P18 Detail of BRTP timing •tPWL: 50ms (max.) → 500ms (max.) •Note5 (addition) P20 Method of connection for LVDS transmitter •Note2 (addition) P21 Display colors and input data signals •This product - gray scales. → This product - 256 gray scale in each R, G, B sub-pixel. P22 Timing characteristics •Note1 (change of expression) P23 Input signal timing chart •CKx+, CKy+ (addition) P26-27 Optics •Luminance: TBD cd/m^2 (min.) → 650cd/m^2 •Luminance uniformity: white(LU) → gray scale (LU0, LU26, LU128, LU204, LU255) •Chromaticity - Rx: TBD (typ.) → 0.650 (typ.) •Chromaticity - Ry: TBD (typ.) → 0.330 (typ.) •Chromaticity - Gx: TBD (typ.) → 0.290 (typ.) •Chromaticity - Gy: TBD (typ.) → 0.610 (typ.) •Chromaticity - Bx: TBD (typ.) → 0.150 (typ.) •Chromaticity - By: TBD (typ.) → 0.060 (typ.) •Color gamut (addition) •Response time- Black to White: 16ms (typ.) →14 ms (typ.) •Response time- White to Black: 11ms (typ.) →10 ms (typ.) •Note3, Note4 (change) P28 Definition of luminance uniformity •Formula: (LU) → (LUxx) •Measured point: 5 points → 9 points P29 Reliability tests •Note2 (addition) P32 Attentions - Characteristics •⑧ (addition) P32 Attentions - Other •④ (addition)

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
2nd edition	DOD-PP-0422	Jan 23, 2008	**Revision contents** P33 Outline drawing - Front view •(12.568) →(12.57) (change) •(11.924) → (11.92) (change) • 1.3±0.5 → 1.5±0.5 (change) P34 Outline drawing - Rear view •Inverter → cover (change) •(42.1) → 41.7 (change) •(290) → 290.8 (change) •2 →(2) (change) **Signature of writer** *Approved by* T. OGAWA *Checked by* —— *Prepared by* E. KATAYAMA