PRELIMINARY

NEC LCD Technologies, Ltd.

TFT MONOCHROME LCD MODULE

NL204153AM21-07A

54cm (21.3 Type)
QXGA
LVDS interface (4 ports)

PRELIMINARY DATA SHEET

DOD-PD-1178 (2nd edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PD-1049(1).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

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INTRODUCTION

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Examples: Control systems for transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, medical equipment not specifically designed for life support, safety equipment, etc.

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL204153AM21-07A is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

- Ultra-wide viewing angle (Adoption of Super-Advanced Super Fine TFT (SA-SFT))
- High luminance
- High contrast
- Low reflection
- High resolution
- 256 gray scales per 1 sub-pixel (8-bit)
- LVDS interface
- Adjustable gamma characteristics by using built-in 10-bit LUT (look up table)
- Selectable LVDS data input map
- Small foot print
- Incorporated direct light type backlight with an inverter
- Replaceable backlight and inverter

2. GENERAL SPECIFICATIONS

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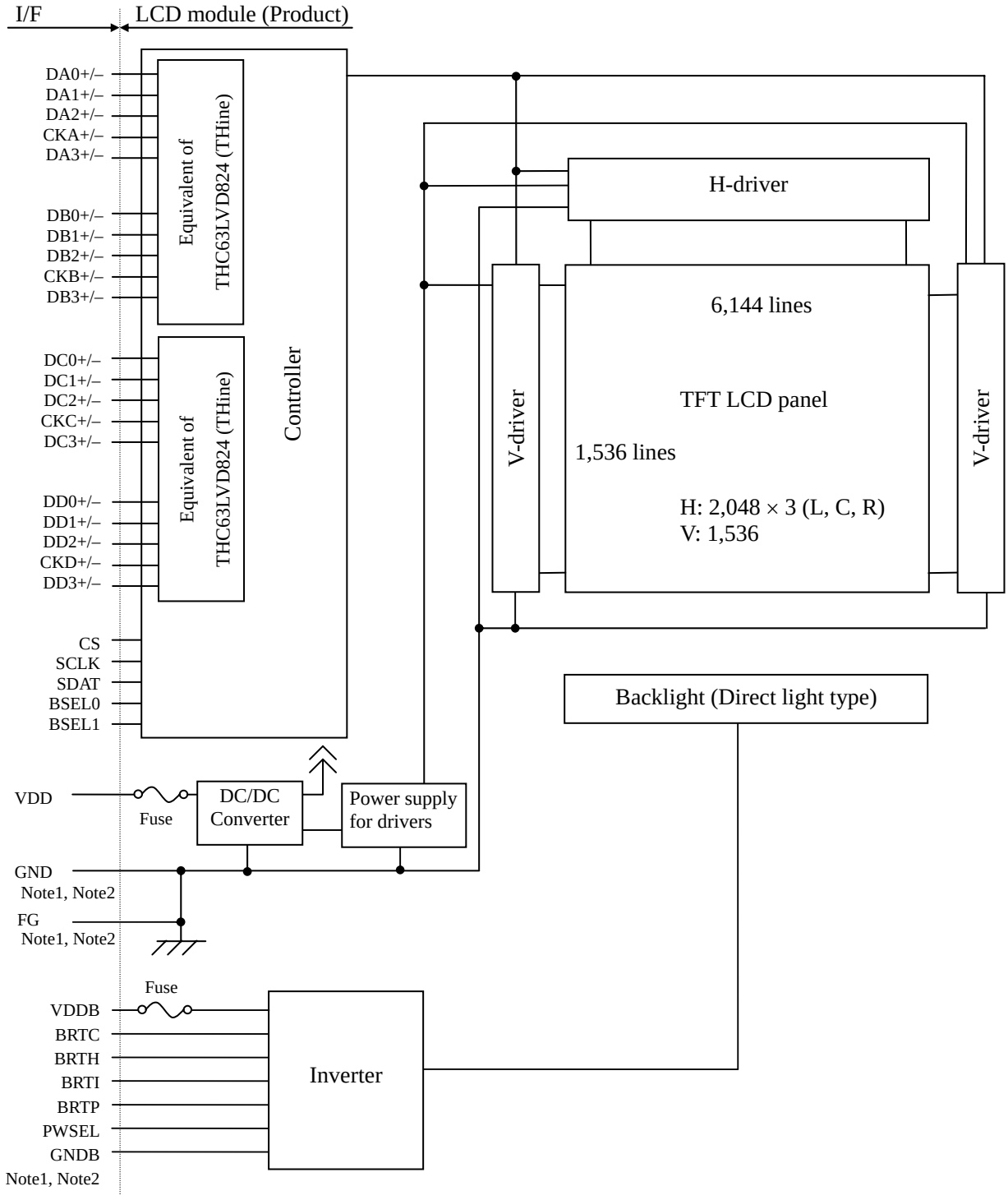
Display area	433.152 (H) × 324.864 (V) mm
Diagonal size of display	54cm (21.3 inches)
Drive system	a-Si TFT active matrix
Display grayscale	256 gray scales per 1 sub-pixel (8-bit) (766 gray scales per 1 pixel)
Pixel	2,048 (H) × 1,536 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)
Pixel arrangement	LCR vertical stripe
Sub-pixel pitch	0.0705 (H) × 0.2115 (V) mm
Pixel pitch	0.2115 (H) × 0.2115 (V) mm
Module size	457.0 (typ., W) × 350.0 (typ., H) × 37.0 (max., D) mm
Weight	3,000g (typ.)
Contrast ratio	700:1 (typ.)
Viewing angle	*At the contrast ratio ≥ 10:1* • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ=DICOM): normal axis (perpendicular) Note1
Polarizer surface	Antiglare
Polarizer pencil-hardness	2H (min.) [by JIS K5400]
Response time	*Ton+Toff (10%←→90%)* 35ms (typ.)
Luminance	*At the maximum luminance control* 1,600cd/m^2 (typ.)
Signal system	4 ports LVDS interface (THC63LVD824×2pcs, THine Electronics, Inc. or equivalent) LCR 8-bit signals, Data enable signal (DE), Dot clock (CLK)
Power supply voltage	LCD panel signal processing board: 12.0V Inverter: 12.0V
Backlight	Direct light type: 16 cold cathode fluorescent lamps with an inverter (Replaceable part • Inverter: 213PW041)
Power consumption	*At checkered flag pattern, the maximum luminance control* 67.2W (typ.)

Note1: When the product luminance is 800cd/m^2, the gamma characteristic is designed to γ=DICOM.

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and GNDB (Inverter ground) in the LCD module

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2 GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

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Parameter	Specification		Unit
Module size	457.0 ± 0.5 (W) × 350.0 ± 0.5 (H) × 37.0 (max., D) Note1	Note2	mm
Display area	433.152 (H) × 324.864 (V)	Note2	mm
Weight	3,000 (typ.), 3,200 (max.)		g

Note1: Excluding warpage of the signal processing board cover and the connection board cover.
Note2: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	-
	Inverter		VDDB	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +2.8	V	VDD= 12.0V
	Inverter	BRTI signal	VBI	-0.3 to +1.5	V	VDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Front surface	TopF	0 to +55	°C	Note2
		Rear surface	TopR	0 to + 60	°C	Note3
Relative humidity Note4			RH	≤ 70	%	Ta ≤ 55°C
Absolute humidity Note4			AH	≤ 73 Note5	g/m^3	Ta > 55°C
Operating altitude			-	≤ 4,850	m	0°C≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C≤ Ta ≤ 60°C

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Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-, CS, SCLK, SDAT, BSEL0, BSEL1
Note2: Measured at center of LCD panel surface (including self-heat)
Note3: Measured at center of LCD module's rear shield surface (including self-heat)
Note4: No condensation
Note5: Water amount at Ta= 55°C and RH= 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	600 Note1	1,100 Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-
Control signal input threshold voltage	High	VIH	High must be Open.			-	Note5
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	
Serial communication signal input threshold voltage	High	V+	-	1.4	1.9	V	Note6
	Low	V-	0.4	0.7	-	V	
	Hysteresis	VH	0.3	-	-	V	

Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS driver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-
Note5: BSEL0, BSEL1
Note6: CS, SCLK, SDAT

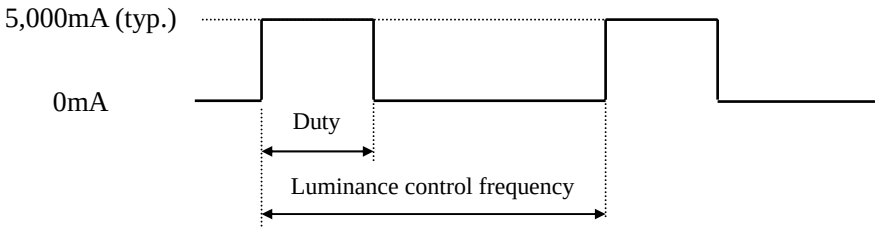
2

4.3.2 Inverter

(Ta= 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage			VDDB	11.4	12.0	12.6	V	-
Power supply current			IDDB	-	5,000	5,700	mA	VDDB= 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0.25	-	1.0	V	-
	BRTP signal	High	VBPH	2.0	-	5.25	V	
		Low	VBPL	0	-	0.8	V	
	BRTC signal	High	VBCH	2.0	-	5.25	V	
		Low	VBCL	0	-	0.8	V	
	PWSEL signal	High	VPSLH	2.0	-	5.25	V	
		Low	VPSLL	0	-	0.8	V	
Input current for signals	BRTI signal		IBI	-200	-	1,000	μA	
	BRTP signal	High	IBPH	-	-	1,000	μA	
		Low	IBPL	-600	-	-	μA	
	BRTC signal	High	IBCH	-	-	400	μA	
		Low	IBCL	-600	-	-	μA	
	PWSEL signal	High	IPSLH	-	-	440	μA	
		Low	IPSLL	-600	-	-	μA	

4.3.3 Inverter current wave



At the maximum luminance control: 100%
At the minimum luminance control: 20%
Luminance control frequency: 255Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of BRTP timing**".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage (See "**4.3.4 Power supply voltage ripple**".) during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

4.3.4 Power supply voltage ripple

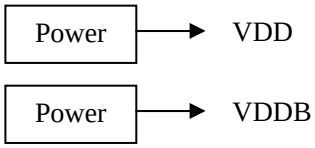
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0V	≤ 100	mVp-p
VDDB	12.0V	≤ 200	mVp-p

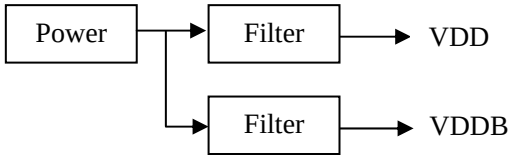
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



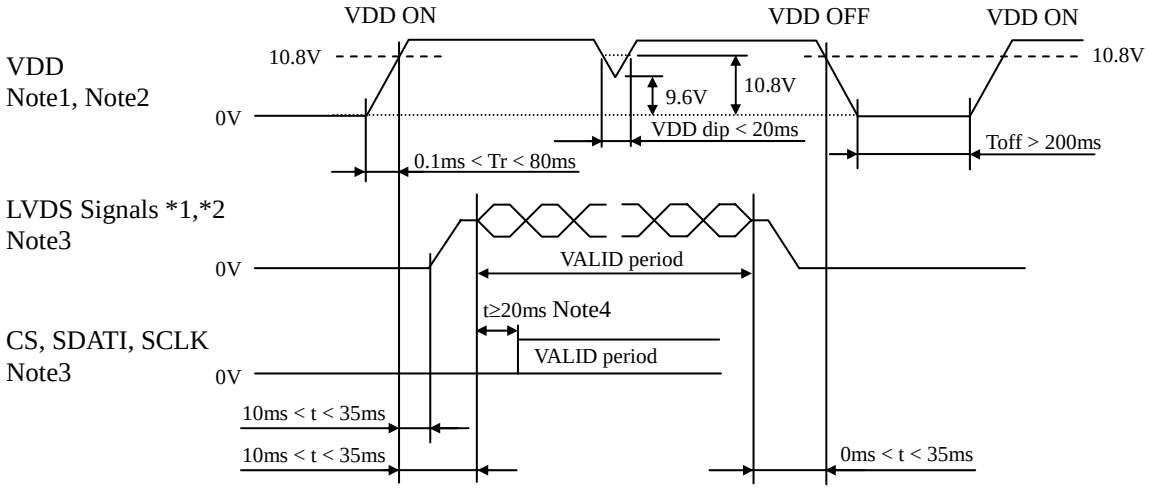
4.3.5 Fuse 2

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202AB	KAMYA ELECTRIC Co., Ltd.	2.0A 32V	4.0A, 5 seconds maximum	Note1
VDDB	R451010	Littelfuse Inc.	10A 125V	20A, 5 seconds maximum	

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-

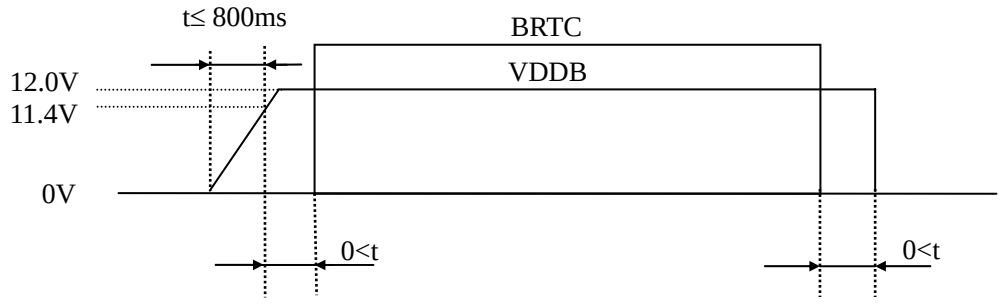
*2: LVDS signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: LVDS signals and CS, SCLK, SDAT must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note3: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input. When writing the LUT data, see "**4.13 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT**".

4.4.2 Inverter



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If tr is more than 800ms, the backlight will be turned off by a protection circuit for inverter.

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

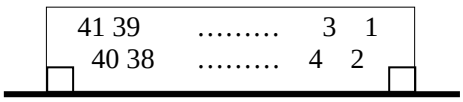
CN1 socket (LCD module side): FI-WE41P-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W41S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	RSVD1	Reserved	Connect to signal ground.
2	N.C.	-	Keep this pin Open.
3	CS	Chip selection (Pull-up 25kΩ)	LUT communication control signal See "**4.13 TEN-bit LOOK UP TABLE FOP GAMMA ADJUSTMENT**".
4	SCLK	Serial Clock (Pull-down 25kΩ)	
5	SDAT	Serial Data (Pull-down 25kΩ)	
6	RSVD2	Reserved	Keep this pin Open.
7			
8	BSEL0	Selection of LVDS data input map (Pull-up 25kΩ)	See "**4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER**". BSEL0 / BSEL1 / Mode Open / Open / A Open / Low / B Low / Open / C Low / Low / A
9	BSEL1		
10	RSVD2	Reserved	Keep this pin Open.
11	GND	Signal ground	Note1
12	DB3+	Pixel data B3	LVDS differential data input Note2
13	DB3-		
14	GND	Signal ground	Note1
15	CKB+	Pixel clock B	LVDS differential clock input Note2
16	CKB-		
17	GND	Signal ground	Note1
18	DB2+	Pixel data B2	LVDS differential data input Note2
19	DB2-		
20	GND	Signal ground	Note1
21	DB1+	Pixel data B1	LVDS differential data input Note2
22	DB1-		
23	GND	Signal ground	Note1
24	DB0+	Pixel data B0	LVDS differential data input Note2
25	DB0-		
26	GND	Signal ground	Note1
27	DA3+	Pixel data A3	LVDS differential data input Note2
28	DA3-		
29	GND	Signal ground	Note1
30	CKA+	Pixel clock A	LVDS differential clock input Note2
31	CKA-		
32	GND	Signal ground	Note1
33	DA2+	Pixel data A2	LVDS differential data input Note2
34	DA2-		
35	GND	Signal ground	Note1
36	DA1+	Pixel data A1	LVDS differential data input Note2
37	DA1-		
38	GND	Signal ground	Note1
39	DA0+	Pixel data A0	LVDS differential data input Note2
40	DA0-		
41	GND	Signal ground	Note1

Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN1: View from insert direction

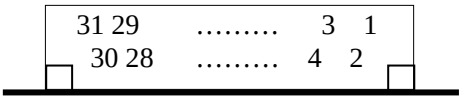


CN2 socket (LCD module side): FI-WE31P-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W31S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Signal ground	Note1
2	DD3+	Pixel data D3	LVDS differential data input Note2
3	DD3-		
4	GND	Signal ground	Note1
5	CKD+	Pixel clock D	LVDS differential clock input Note2
6	CKD-		
7	GND	Signal ground	Note1
8	DD2+	Pixel data D2	LVDS differential data input Note2
9	DD2-		
10	GND	Signal ground	Note1
11	DD1+	Pixel data D1	LVDS differential data input Note2
12	DD1-		
13	GND	Signal ground	Note1
14	DD0+	Pixel data D0	LVDS differential data input Note2
15	DD0-		
16	GND	Signal ground	Note1
17	DC3+	Pixel data C3	LVDS differential data input Note2
18	DC3-		
19	GND	Signal ground	Note1
20	CKC+	Pixel clock C	LVDS differential clock input Note2
21	CKC-		
22	GND	Signal ground	Note1
23	DC2+	Pixel data C2	LVDS differential data input Note2
24	DC2-		
25	GND	Signal ground	Note1
26	DC1+	Pixel data C1	LVDS differential data input Note2
27	DC1-		
28	GND	Signal ground	Note1
29	DC0+	Pixel data C0	LVDS differential data input Note2
30	DC0-		
31	GND	Signal ground	Note1

Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN2: View from insert direction



CN3 socket (LCD module side): IL-Z-8PL-SMTY (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-8S-S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	Note1
2	VDD		
3	VDD		
4	VDD		
5	GND	Signal ground	Note1
6	GND		
7	GND		
8	GND		

Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 Inverter

CN201 socket (LCD module side): DF3-10P-2H (20/21) (HIROSE ELECTRIC Co., Ltd. (HRS))
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co., Ltd. (HRS))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

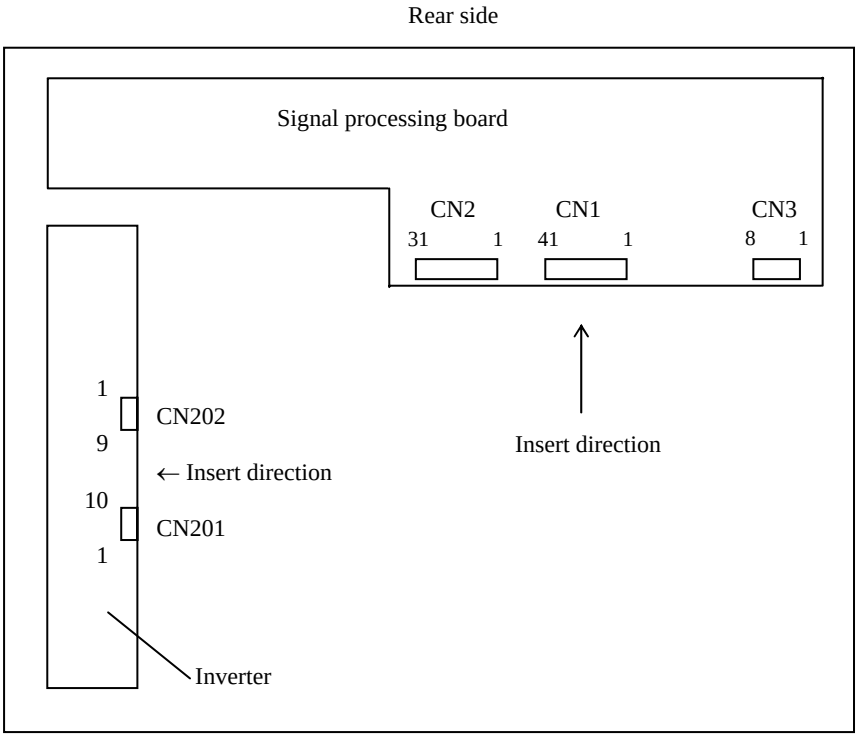
Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTY (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control signal	Note2
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	Inverter ground	Note1
9	PWSEL	Selection of luminance control method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: See "**4.6.1 Luminance control methods**".
Note3: In case VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket

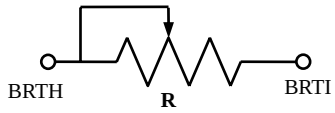


4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL terminal</th><th>BRTP terminal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment

The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.
The resistor (R) must be connected between BRTH-BRTI terminals.
 

• Luminance ratio Note3
<table>
<tr><th>Resistance</th><th>Luminance ratio</th></tr>
<tr><td>1.5kΩ Note4</td><td>20% (Min. Luminance)</td></tr>
<tr><td>10kΩ</td><td>100% (Max. Luminance)</td></tr>
</table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment

Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.
Luminance is the maximum when BRTI terminal is Open.

• Luminance ratio Note3
<table>
<tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr>
<tr><td>0.25V Note4</td><td>20% (Min. Luminance)</td></tr>
<tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr>
</table></td></tr>
<tr><td>Pulse width modulation

Note1
Note2
Note5</td><td>• Adjustment

Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.

• Luminance ratio Note3
<table>
<tr><th>Duty ratio Note4</th><th>Luminance ratio</th></tr>
<tr><td>0.2</td><td>20% (Min. Luminance)</td></tr>
<tr><td>1.0</td><td>100% (Max. Luminance)</td></tr>
</table></td><td>Low</td><td>BRTP signal</td></tr>
</table>

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.
Use PWM method, if interference noises appear on the display image!

Note2: The inverter will stop working, when BRTP signal is fixed to Low while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. Backlight inverter will start to work when power is supplied again.

Note3: These data are the target values.

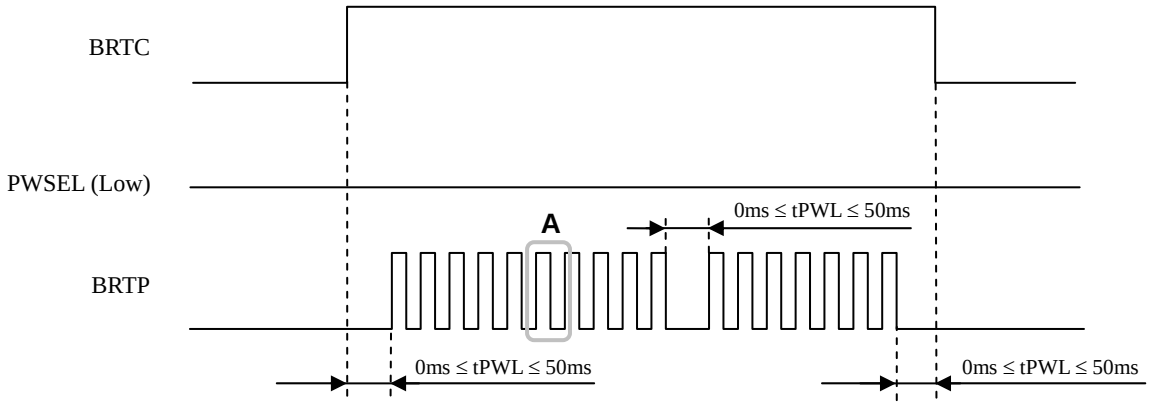
Note4: Do not set the variable resistor and BRTI voltage in less than 1.5kΩ or less than 0.25V. Otherwise flicker or display mura may cause, or the lamp may not be turned on.

Note5: See "**4.6.2 Detail of BRTP timing**".

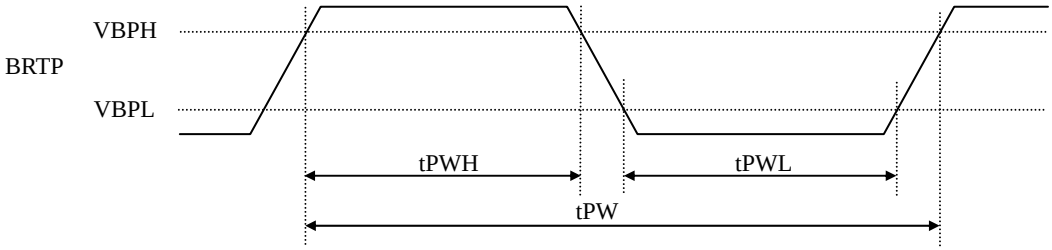
4.6.2 Detail of BRTP timing

(1) Timing diagrams

- Outline chart



- Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	185	-	325	Hz	Note1, Note2
Duty ratio	DL	0.2	-	1.0	-	Note1, Note3
Low period	tPWL	0	-	50	ms	Note4

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW}, \quad DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.

Luminance control frequency= 1/tv × (n+0.25) [or (n+0.75)]
n = 1, 2, 3 · · · · · ·
tv: Vertical cycle (See "**4.9.1 Timing characteristics**".)

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "**4.6.1 Luminance control methods**".

Note4: If tPWL is more than 50ms, the backlight will be turned off by a protection circuit for inverter. The inverter will start to work when power is supplied again.

4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER

LVDS data input map is selectable by BSEL0 and BSEL1 terminal.

	Bit mapping			Transmitter Pin Assignment					CN1	
	BSEL[1:0] Note1			Single type LVDS Tx	Dual type LVDS TX		Output Connector		Pin No.	Signal name
	[H:H], [L:L] Mode A	[H:L] Mode B	[L:H] Mode C		THine THC63LVD823	NS DS90C387				
Pixel data A	LA2	LA7	LA0	TA0	R12	R10				
	LA3	LA6	LA1	TA1	R13	R11		Note2		
	LA4	LA5	LA2	TA2	R14	R12	ATA-	→	40	DA0-
	LA5	LA4	LA3	TA3	R15	R13	ATA+	→	39	DA0+
	LA6	LA3	LA4	TA4	R16	R14				
	LA7	LA2	LA5	TA5	R17	R15				
	CA2	CA7	CA0	TA6	G12	G10				
	CA3	CA6	CA1	TB0	G13	G11				
	CA4	CA5	CA2	TB1	G14	G12				
	CA5	CA4	CA3	TB2	G15	G13	ATB-	→	37	DA1-
	CA6	CA3	CA4	TB3	G16	G14	ATB+	→	36	DA1+
	CA7	CA2	CA5	TB4	G17	G15				
	RA2	RA7	RA0	TB5	B12	B10				
	RA3	RA6	RA1	TB6	B13	B11				
	RA4	RA5	RA2	TC0	B14	B12				
	RA5	RA4	RA3	TC1	B15	B13				
	RA6	RA3	RA4	TC2	B16	B14	ATC-	→	34	DA2-
	RA7	RA2	RA5	TC3	B17	B15	ATC+	→	33	DA2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LA0	LA1	LA6	TD0	R10	R16				
	LA1	LA0	LA7	TD1	R11	R17				
	CA0	CA1	CA6	TD2	G10	G16	ATD-	→	28	DA3-
	CA1	CA0	CA7	TD3	G11	G17	ATD+	→	27	DA3+
	RA0	RA1	RA6	TD4	B10	B16				
	RA1	RA0	RA7	TD5	B11	B17				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	ATCLK-	→	31	CKA-
							ATCLK+	→	30	CKA+
Pixel data B	LB2	LB7	LB0	TA0	R22	R20				
	LB3	LB6	LB1	TA1	R23	R21				
	LB4	LB5	LB2	TA2	R24	R22	BTA-	→	25	DB0-
	LB5	LB4	LB3	TA3	R25	R23	BTA+	→	24	DB0+
	LB6	LB3	LB4	TA4	R26	R24				
	LB7	LB2	LB5	TA5	R27	R25				
	CB2	CB7	CB0	TA6	G22	G20				
	CB3	CB6	CB1	TB0	G23	G21				
	CB4	CB5	CB2	TB1	G24	G22				
	CB5	CB4	CB3	TB2	G25	G23	BTB-	→	22	DB1-
	CB6	CB3	CB4	TB3	G26	G24	BTB+	→	21	DB1+
	CB7	CB2	CB5	TB4	G27	G25				
	RB2	RB7	RB0	TB5	B22	B20				
	RB3	RB6	RB1	TB6	B23	B21				
	RB4	RB5	RB2	TC0	B24	B22				
	RB5	RB4	RB3	TC1	B25	B23				
	RB6	RB3	RB4	TC2	B26	B24	BTC-	→	19	DB2-
	RB7	RB2	RB5	TC3	B27	B25	BTC+	→	18	DB2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LB0	LB1	LB6	TD0	R20	R26				
	LB1	LB0	LB7	TD1	R21	R27				
	CB0	CB1	CB6	TD2	G20	G26	BTD-	→	13	DB3-
	CB1	CB0	CB7	TD3	G21	G27	BTD+	→	12	DB3+
	RB0	RB1	RB6	TD4	B20	B26				
	RB1	RB0	RB7	TD5	B21	B27				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	BTCLK-	→	16	CKB-
							BTCLK+	→	15	CKB+

	BSEL[1:0] Note1			Single type LVDS Tx	Dual type LVDS TX		Output Connector		CN2	
	[H:H], [L:L] Mode A	[H:L] Mode B	[L:H] Mode C		THine THC63LVD823	NS DS90C387			Pin No.	Signal name
Pixel data C	LC2	LC7	LC0	TA0	R12	R10				
	LC3	LC6	LC1	TA1	R13	R11		Note2		
	LC4	LC5	LC2	TA2	R14	R12	CTA-	→	30	DC0-
	LC5	LC4	LC3	TA3	R15	R13	CTA+	→	29	DC0+
	LC6	LC3	LC4	TA4	R16	R14				
	LC7	LC2	LC5	TA5	R17	R15				
	CC2	CC7	CC0	TA6	G12	G10				
	CC3	CC6	CC1	TB0	G13	G11				
	CC4	CC5	CC2	TB1	G14	G12				
	CC5	CC4	CC3	TB2	G15	G13	CTB-	→	27	DC1-
	CC6	CC3	CC4	TB3	G16	G14	CTB+	→	26	DC1+
	CC7	CC2	CC5	TB4	G17	G15				
	RC2	RC7	RC0	TB5	B12	B10				
	RC3	RC6	RC1	TB6	B13	B11				
	RC4	RC5	RC2	TC0	B14	B12				
	RC5	RC4	RC3	TC1	B15	B13				
	RC6	RC3	RC4	TC2	B16	B14	CTC-	→	24	DC2-
	RC7	RC2	RC5	TC3	B17	B15	CTC+	→	23	DC2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LC0	LC1	LC6	TD0	R10	R16				
	LC1	LC0	LC7	TD1	R11	R17				
	CC0	CC1	CC6	TD2	G10	G16	CTD-	→	18	DC3-
	CC1	CC0	CC7	TD3	G11	G17	CTD+	→	17	DC3+
	RC0	RC1	RC6	TD4	B10	B16				
	RC1	RC0	RC7	TD5	B11	B17				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	CTCLK-	→	21	CKC-
							CTCLK+	→	20	CKC+
Pixel data D	LD2	LD7	LD0	TA0	R22	R20				
	LD3	LD6	LD1	TA1	R23	R21				
	LD4	LD5	LD2	TA2	R24	R22	DTA-	→	15	DD0-
	LD5	LD4	LD3	TA3	R25	R23	DTA+	→	14	DD0+
	LD6	LD3	LD4	TA4	R26	R24				
	LD7	LD2	LD5	TA5	R27	R25				
	CD2	CD7	CD0	TA6	G22	G20				
	CD3	CD6	CD1	TB0	G23	G21				
	CD4	CD5	CD2	TB1	G24	G22				
	CD5	CD4	CD3	TB2	G25	G23	DTB-	→	12	DD1-
	CD6	CD3	CD4	TB3	G26	G24	DTB+	→	11	DD1+
	CD7	CD2	CD5	TB4	G27	G25				
	RD2	RD7	RD0	TB5	B22	B20				
	RD3	RD6	RD1	TB6	B23	B21				
	RD4	RD5	RD2	TC0	B24	B22				
	RD5	RD4	RD3	TC1	B25	B23				
	RD6	RD3	RD4	TC2	B26	B24	DTC-	→	9	DD2-
	RD7	RD2	RD5	TC3	B27	B25	DTC+	→	8	DD2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LD0	LD1	LD6	TD0	R20	R26				
	LD1	LD0	LD7	TD1	R21	R27				
	CD0	CD1	CD6	TD2	G20	G26	DTD-	→	3	DD3-
	CD1	CD0	CD7	TD3	G21	G27	DTD+	→	2	DD3+
	RD0	RD1	RD6	TD4	B20	B26				
	RD1	RD0	RD7	TD5	B21	B27				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	DTCLK-	→	6	CKD-
							DTCLK+	→	5	CKD+

Note1: High must be Open.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

4.8 DISPLAY GRAY SCALE AND INPUT DATA SIGNALS

This product can display 256 gray scales in each LCR sub-pixel and 766 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display gray scale		Data signal (0: Low level, 1: High level)																											
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
		LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
		LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

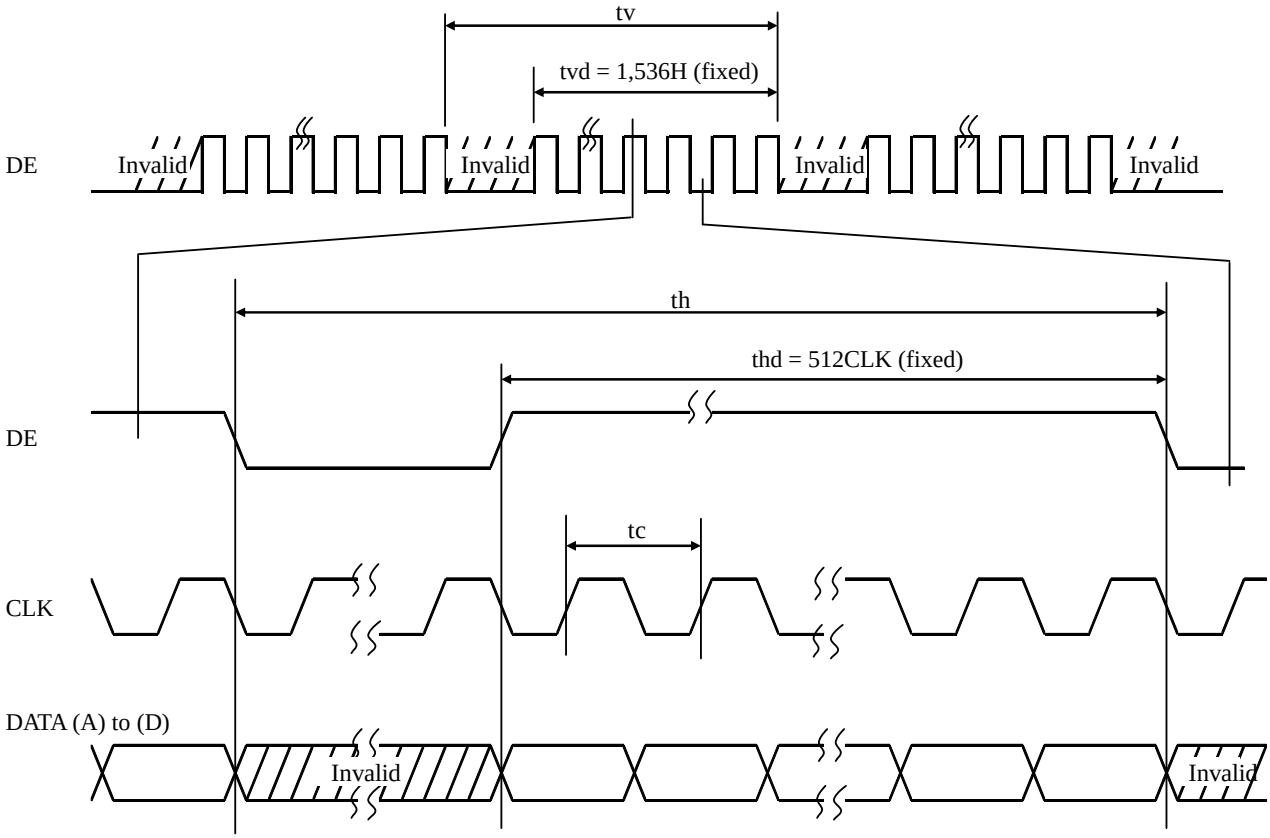
4.9 INPUT SIGNAL TIMINGS

4.9.1 Timing characteristics

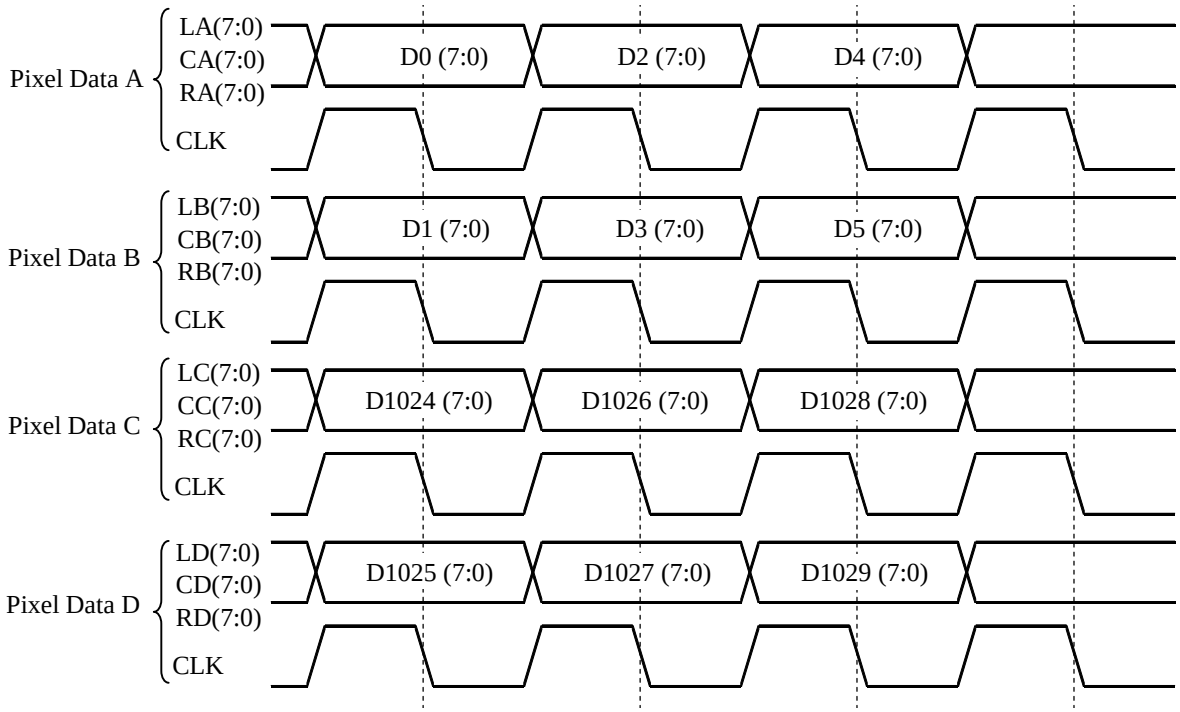
Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/ tc	60.0	65.0	66.0	MHz	15.38ns (typ.)
	Duty		-	See the data sheet of LVDS transmitter.			-	-
	Rise time, Fall time		-				ns	-
DE	Horizontal	Cycle	th	10.34	10.34	10.77	µs	96.72kHz (typ.) Note1
				640	672	700	CLK	
		Display period	thd	512			CLK	-
	Vertical	Cycle	tv	15.47	16.667	17.9	ms	60.0Hz (yp.)
				1,547	1,612	1,628	H	
		Display period	tvd	1,536			H	-
	CLK-DE	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-
DATA (A) to (D)	CLK-DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-

Note1: The sum of jitter and skew of horizontal period should be within ±1 CLK.

4.9.2 Input signal timing chart



4.10 LVDS DATA TARANSMISSION METHOD



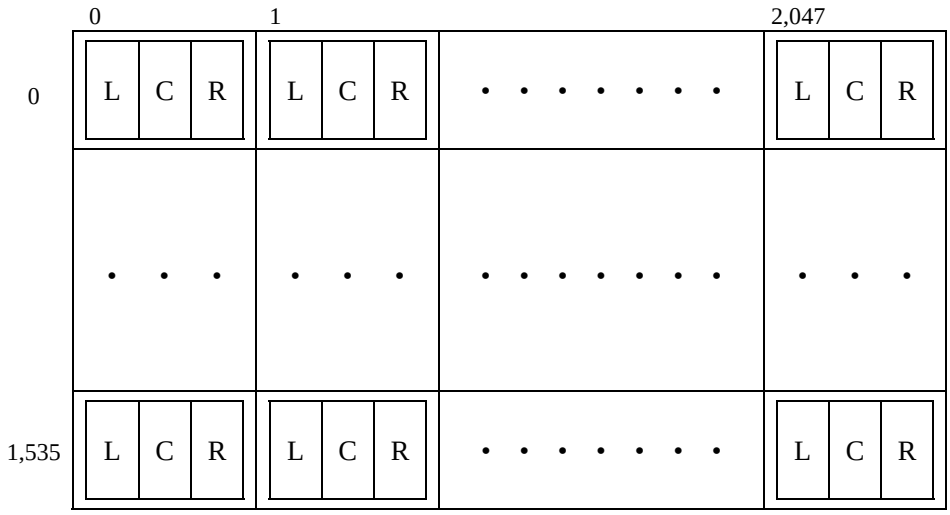
4.11 DISPLAY POSITIONS

D (0, 0)			D (1, 0)		
LA	CA	RA	LB	CB	RB

D (1024, 0)			D (1025, 0)		
LC	CC	RC	LD	CD	RD

0, 0	1, 0	• • •	1022, 0	1023, 0	1024, 0	1025, 0	• • •	2046, 0	2047, 0
0, 1	1, 1	• • •	1022, 1	1023, 1	1024, 1	1025, 1	• • •	2046, 1	2047, 1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0, 1534	1, 1534	• • •	1022, 1534	1023, 1534	1024, 1534	1025, 1534	• • •	2046, 1534	2047, 1534
0, 1535	1, 1535	• • •	1022, 1535	1023, 1535	1024, 1535	1025, 1535	• • •	2046, 1535	2047, 1535

4.12 PIXEL ARRANGNMENT



4.13 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics for each 8-bit LCR data is possible by using built-in 10-bit LUT (look up table) for Gamma characteristics.

The LUT is set with the serial data. The combination of the control command determines Random/Sequential Address WRITE and Individual/Simultaneous LCR setting.

The serial data is composed as Table1.

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See Table2 and 3.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See Table4.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	
D15	DATA15	LUT Data (MSB)	See Table5.
D14	DATA14	LUT Data	
D13	DATA13	LUT Data	
D12	DATA12	LUT Data	
D11	DATA11	LUT Data	
D10	DATA10	LUT Data	
D9	DATA9	LUT Data	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

Table2: Command table (CMD5 to CMD0: 6-bit)

DATA name	Parameter	Remarks
CMD5	Must be set to "1".	-
CMD4	Must be set to "1".	-
CMD3	Selection of Random/Sequential Address WRITE "1": Random Address WRITE "0": Sequential Address WRITE	-
CMD2	Must be set to "1".	-
CMD1	Selection of Individual/Simultaneous LCR setting "1": Individual LCR setting "0": Simultaneous LCR setting	"1": Select the Sub-pixel by using ADD9 and ADD8. (See Table4.) "0": ADD9 and ADD8 are invalid.
CMD0	Must be set to "0".	-

Table3: Command table (CMD5 to CMD0: 6-bit)

CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Function
1	1	1	1	1	0	Random Address WRITE, Individual LCR setting
1	1	1	1	0	0	Random Address WRITE, Simultaneous LCR setting
1	1	0	1	1	0	Sequential Address WRITE, Individual LCR setting
1	1	0	1	0	0	Sequential Address WRITE, Simultaneous LCR setting

*Other combinations are prohibited, and may cause function error.

Table4: Address table (ADD9 to ADD0: 10-bit)

DATA name	Parameter	Remarks
ADD9 ADD8	Sub-pixel Selection ADD[9:8]= 0:0 Left Sub-pixel 0:1 Center Sub-pixel 1:0 Right Sub-pixel 1:1 ON/OFF selection of Gamma Correction	When "ADD[9:8]=1:1", ON/OFF of Gamma correction can select according to the GMA[2:0]. (See Table6 and Table7.)
ADD7 ADD6 ADD5 ADD4 ADD3 ADD2 ADD1 ADD0	LUT Address 256 address = 00h - FFh	When "ADD[9:8] = 1:1", ADD[7:0] must be set to 00h.

Table5: Data table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	DATA9	[MSB]	-
DATA8	DATA8		
DATA7	DATA7		
DATA6	DATA6		
DATA5	DATA5	10-bit LUT Data 000h - 3FFh	
DATA4	DATA4		
DATA3	DATA3		
DATA2	DATA2		
DATA1	DATA1		
DATA0	DATA0	[LSB]	

Table6: Gamma correction table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	Dummy		
DATA8	Dummy		
DATA7	Dummy		
DATA6	Dummy		
DATA5	Dummy		
DATA4	Dummy		
DATA3	Dummy		
DATA2	GAM2	[MSB]	See Table7.
DATA1	GAM1	GMA Data	
DATA0	GAM0	[LSB]	

Table7: Control code GAM[2:0]

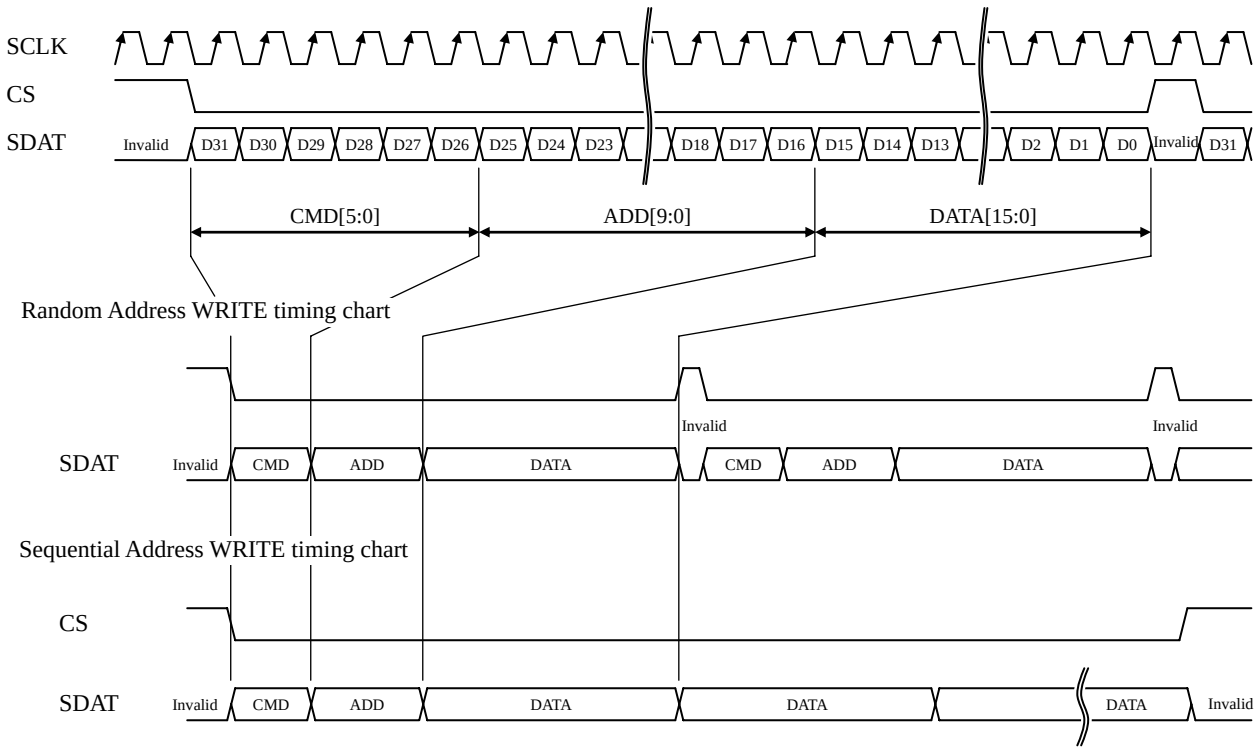
GMA2	GMA1	GMA0	Function
0	0	0	No correction (Initial setting)
0	0	1	Correction according to the LUT Data. Note1

*Other combinations are prohibited, and may cause function error.

Note1: Initial setting of the LUT is undefined data. The LUT should be enabled by setting of the GMA after writing the LUT data in all the 256 addresses, in order to avoid undefined data display.
Note2: Transfer the data every power-on, because the LUT data isn't stored in the LCD module.
Note3: As writing the LUT data, a noise may appear on the display image. In order to prevent the noise appearing on the display, following measures should be performed.
(1) The LUT data should be rewritten during invalid period of pixel data (See "**4.9 INPUT SIGNAL TIMINGS**".).
(2) The LUT data should be rewritten when the Gamma Correction is OFF (GMA[2:0] = 000).

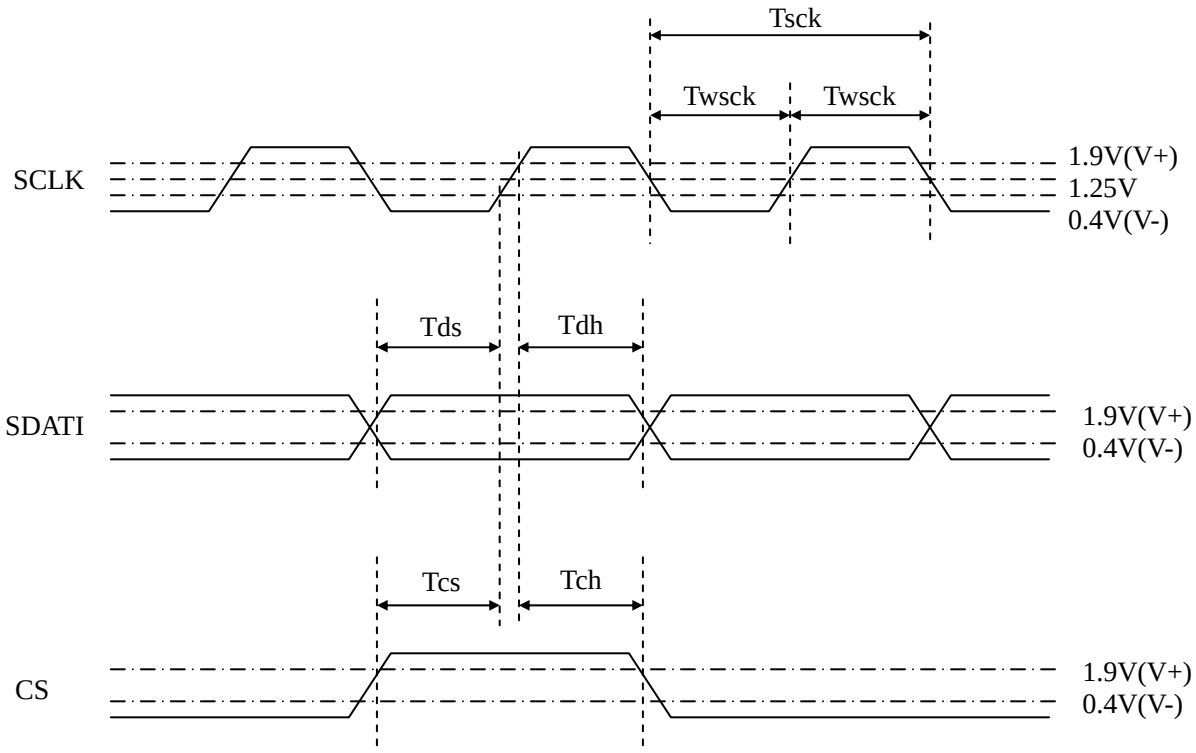
4.14 LUT SERIAL COMMUCATION TIMINGS

(1) Timing chart



(2) Timing specifications

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
SCLK Frequency	1/Tsck	-	-	5	MHz	-
SCLK Pulse	Twsck	50	-	-	ns	-
SDAT-SCLK Setup Time	Tds	50	-	-	ns	-
SDAT-SCLK Hold Time	Tdh	50	-	-	ns	-
CS-SCLK Setup Time	Tcs	50	-	-	ns	-
CS-SCLK Hold Time	Tch	50	-	-	ns	-



Note1: During the serial communication mode, the display noise may appear because of rewriting the data. To avoid this, rewrite the LUT data when the pixel data is invalid or the Gamma Correction is OFF (GMA[2:0] = 000). The external noise may cause the data change, refresh the data regularly according to need.

4.15 OPTICS

4.15.1 Optical characteristics

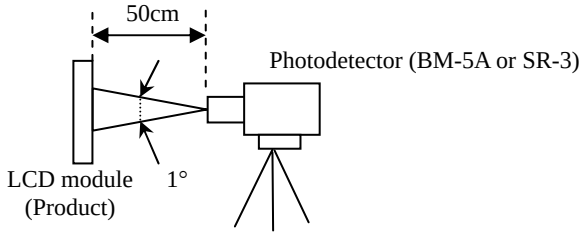
(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	TBD	1,600	-	cd/m^2	BM-5A or SR-3	-
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	450	700	-	-	BM-5A or SR-3	Note3
Luminance uniformity		White θR= 0°, θL= 0°, θU= 0°, θD= 0°	LU	-	1.15	1.3	-	BM-5A	Note4
Chromaticity	White	**x** coordinate	Wx	-	0.280	-	-	SR-3	Note5
		y coordinate	Wy	-	0.304	-	-		
Response time		Black to White	Ton	-	17	25	ms	BM-5A	Note6 Note7
		White to Black	Toff	-	18	25	ms		
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	70	85	-	°	BM-5A	Note8
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	70	85	-	°		
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	70	85	-	°		
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	70	85	-	°		

2

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
Ta= 25°C, VDD= 12.0V, VDDB= 12.0V, Display mode: QXGA,
Horizontal cycle= 1/96.72kHz, Vertical cycle= 1/60.0Hz

Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note3: See "**4.15.2 Definition of contrast ratio**".
Note4: See "**4.15.3 Definition of luminance uniformity**".
Note5: These coordinates are found on CIE 1931 chromaticity diagram.
Note6: Product surface temperature: TopF= 35°C
Note7: See "**4.15.4 Definition of response times**".
Note8: See "**4.15.5 Definition of viewing angles**".

4.15.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

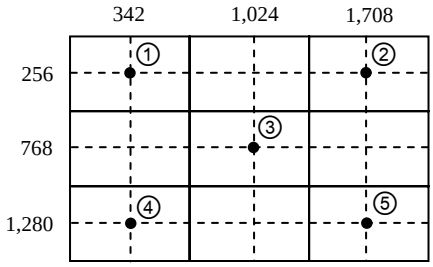
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.15.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

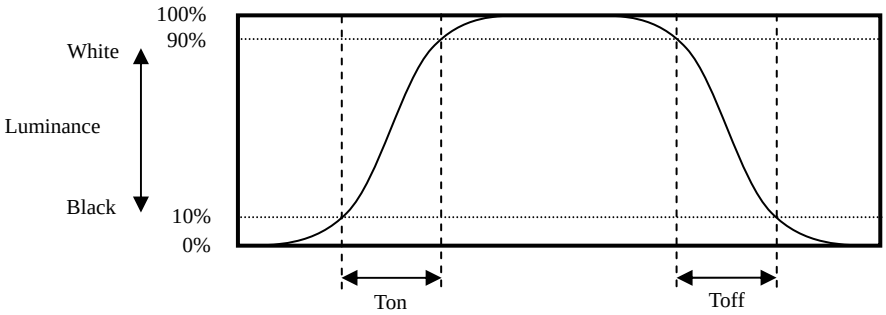
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

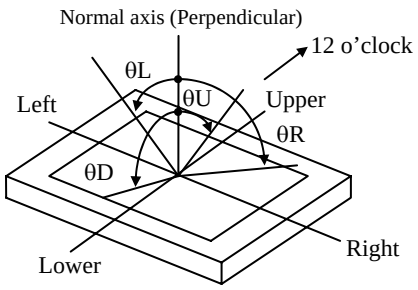


4.15.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.15.5 Definition of viewing angles

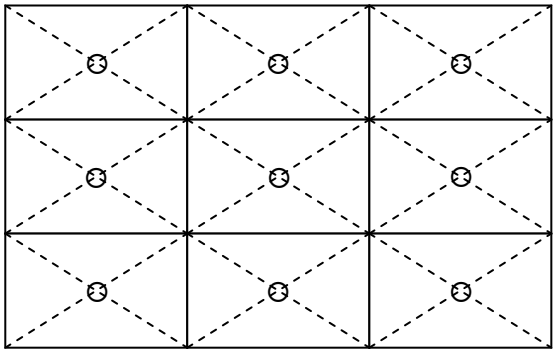


5. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH= 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	Non-operation	① 15kPa (Equivalent to altitude 13,600m) ② -20°C±3°C…24 hours ③ +60°C±3°C…24 hours	No display malfunctions
	Operation	① 53.3kPa (Equivalent to altitude 4,850m) ② 0°C±3°C…24 hours ③ +55°C±3°C…24 hours	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points

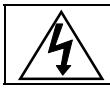


6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.



This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

- **Do not touch the working backlight. There is a danger of an electric shock.**

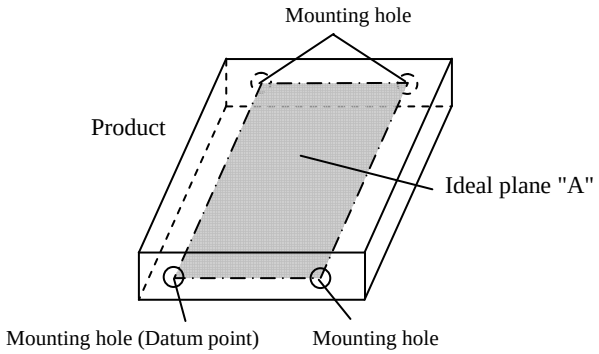
- **Do not touch the working backlight. There is a danger of burn injury.**
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N (ϕ16mm jig))**

6.3 ATTENTIONS 

6.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed 0.735N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 4.7mm.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
⑧ Do not push nor pull the interface connectors while the product is working.
⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

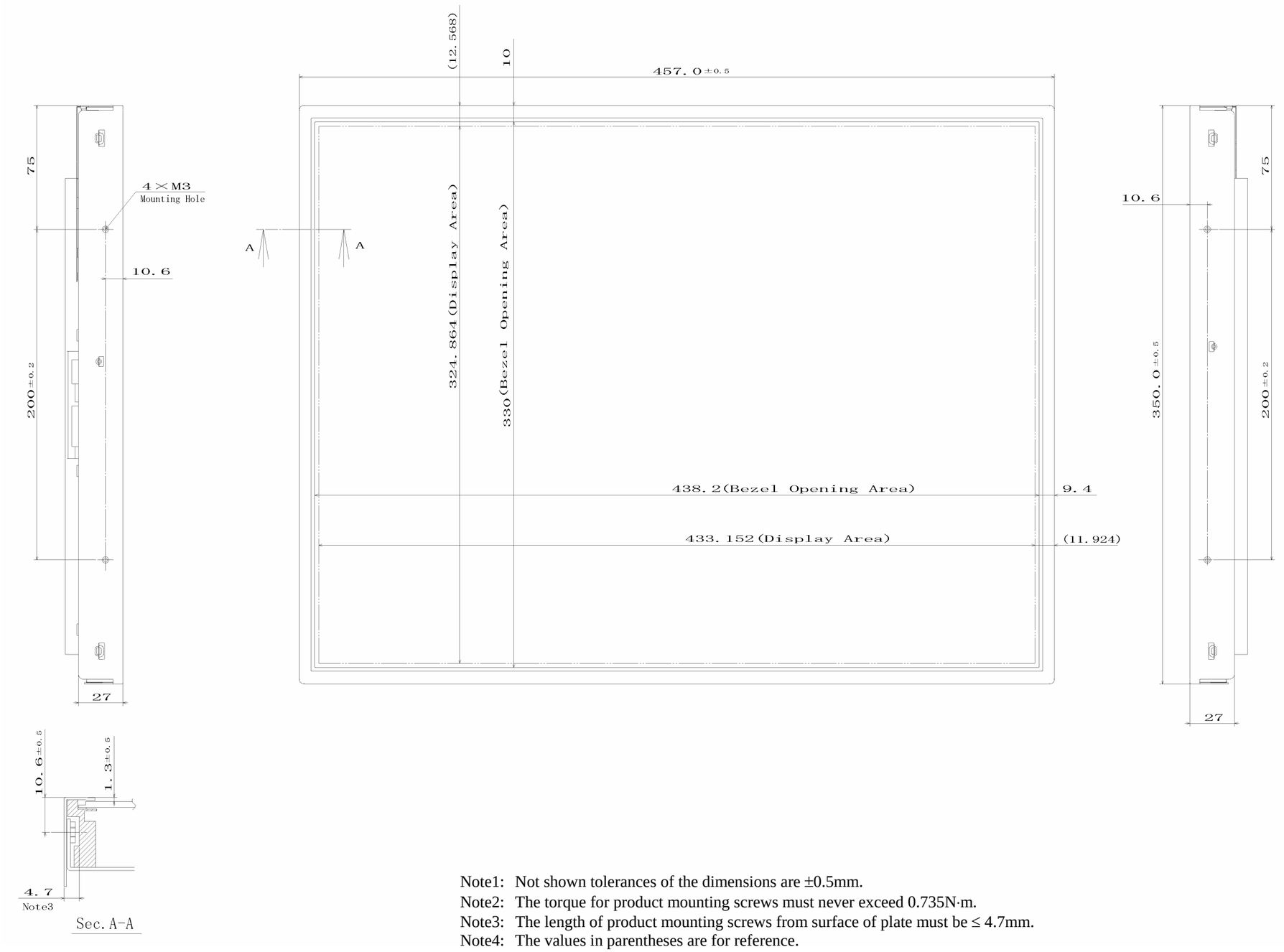
① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed depending on input signal timings.
⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

6.3.4 Other

① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ See "REPLACEMENT MANUAL FOR INVERTER", when replacing backlight lamps.
④ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

7. OUTLINE DRAWINGS

7.1 FRONT VIEW

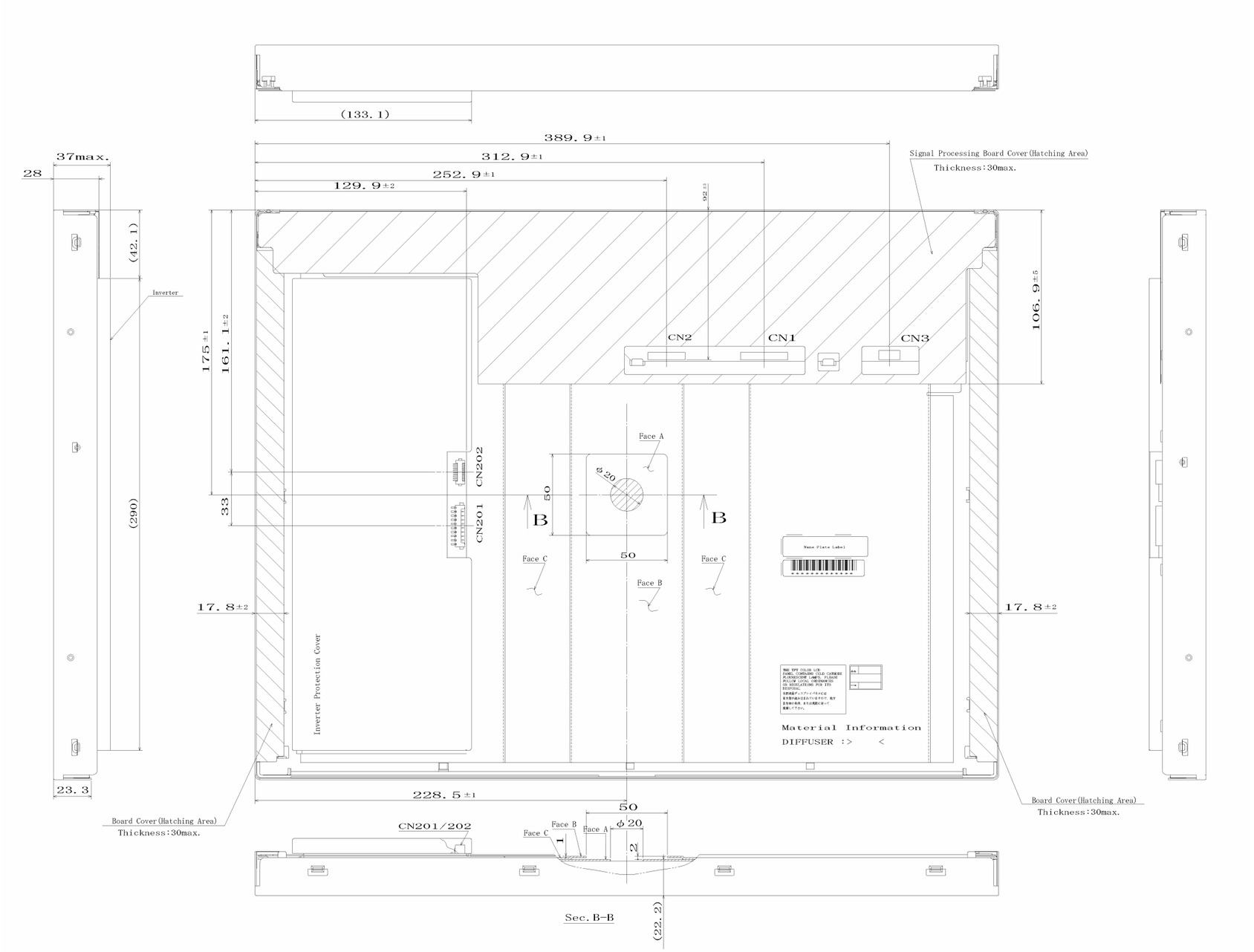


Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 4.7mm.
Note4: The values in parentheses are for reference.

Unit: mm

2

7.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The values in parentheses are for reference.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PD-1049	June 17, 2005	**Revision contents** New issue **Writer** *Approved by* T. ITO *Checked by* ——— *Prepared by* R. KAWASHIMA
2nd edition	DOD-PD-1178	Oct. 7, 2005	**Revision contents** Data correction or implementation depend on the specification review P4 General specifications P7 Mechanical specifications, Absolute maximum ratings P9 Electrical characteristics- Inverter P10 Fuse- VDDB P11 Power supply voltage sequence P29 Optical characteristics- Response time P35, P36 Outline drawings **Signature of writer** *Approved by* T. ITO *Checked by* ——— *Prepared by* R. KAWASHIMA