PRELIMINARY

NEC LCD Technologies, Ltd.

TFT MONOCHROME LCD MODULE

NL280210AM15-01

54cm (21.3 Type)
QSXGA+
LVDS Interface (4 ports)

PRELIMINARY DATA SHEET

DOD-PP-0006 (3rd edition)

This PRELIMINARY DATA SHEET is updated document from DOD-MD-0073(2).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

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INTRODUCTION

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL280210AM15-01 are composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

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- Ultra-wide viewing angle (Adoption of Super-Advanced Super Fine TFT (SA-SFT))
- High luminance
- High contrast
- Low reflection
- High resolution
- 1,024 gray scales per 1 sub-pixel (10-bit)
- LVDS interface
- Small foot print
- Incorporated direct type backlight with an inverter

2. GENERAL SPECIFICATIONS

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Display area	432.6 (H) × 324.5 (V) mm
Diagonal size of display	54 cm (21.3 inches)
Drive system	a-Si TFT active matrix
Display gray scale	1,024 gray scales per 1 sub-pixel (10-bit) (3,072 gray scales per 1 pixel)
Pixel	2,800 (H) × 2,100 (V) pixels (1 pixel consists of 3 sub pixels (LCR))
Pixel arrangement	LCR Vertical stripe
Sub-pixel pitch	0.051 (H) × 0.154 (V) mm
Pixel pitch	0.154 (H) × 0.154 (V) mm
Module size	(457.0) (W) × (350.0) (H) × (39.6) (D) mm (typ.)
Weight	(3,500) g (typ.)
Contrast ratio	(1,000:1) (typ.)
Viewing angle	*At the contrast ratio ≥10:1* • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ=DICOM): normal axis (perpendicular) Note1
Polarizer surface	Antiglare
Polarizer pencil-hardness	4H (min.) [by JIS K5400]
Response time	*Ton + Toff (10%←→ 90%)* TBD ms (typ.)
Luminance	*At the maximum luminance control* (1,000) cd/m^2 (typ.)
White chromaticity	Wx, Wy = (0.299, 0.315) (typ.)
Signal system	4 ports LVDS interface (THC63LVD104S×4pcs, THine Electronics, Inc. or equivalent) [LCR 10-bit signals, Data enable signal (DE), Dot clock (CLK)]
Power supply voltage	LCD panel signal processing board: 12.0V Inverter: 12.0V
Backlight	Direct light type: 16 cold cathode fluorescent lamp with an inverter
Power consumption	*At checkered flag pattern, the maximum luminance control* (71) W (typ.)

Note1: When the product luminance is 500cd/m^2, the gamma characteristic is designed to γ=DICOM.

3. BLOCK DIAGRAM

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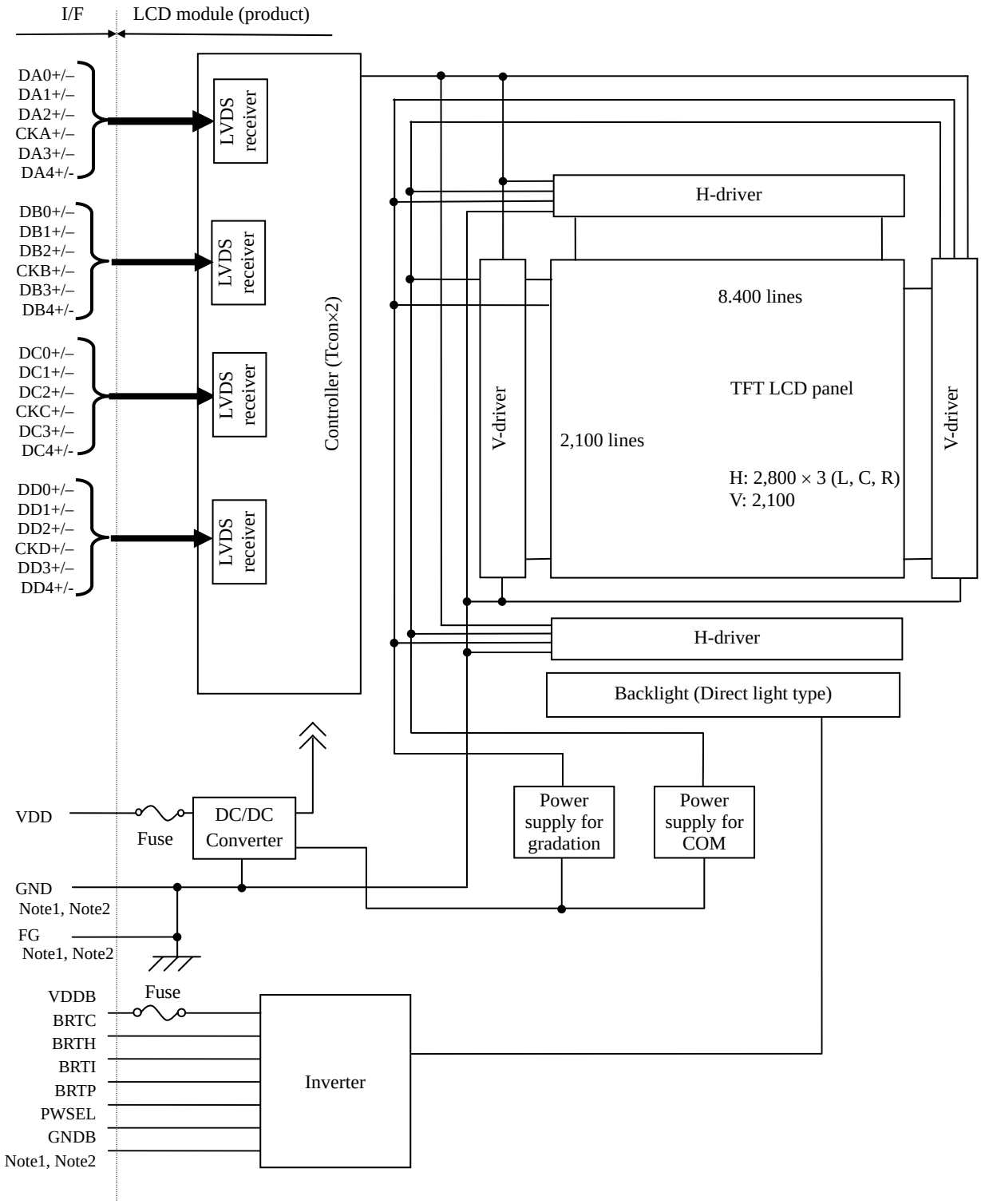

Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (Inverter ground) in the LCD module are as follows.

GND - FG	Connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that these grounds are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

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4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	(457.0) (W) × (350.0) (H) × (39.6) (D)(typ.)	Note1	mm
Display area	432.6 (H) × 324.5 (V)	Note1	mm
Weight	(3,500) (typ.)		g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	-
	Inverter		VDDB	-0.3 to (+15.0)	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to (+2.8)	V	VDD = 12.0V
	Inverter	BRTI signal	VBI	-0.3 to (+1.5)	V	VDDB = 12.0V
		BRTP signal	VBP	-0.3 to (+5.5)	V	
		BRTC signal	VBC	-0.3 to (+5.5)	V	
		PWSEL signal	VBS	-0.3 to (+5.5)	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Front surface	TopF	0 to +55	°C	Note2
		Rear surface	TopR	0 to + 60	°C	Note3
Relative humidity Note4			RH	≤ 70	%	Ta ≤ 55°C
Absolute humidity Note4			AH	≤ 73 Note5	g/m^3	Ta > 55°C
Operating altitude			-	≤ 4,850	m	0°C ≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

Note2: Measured at center of LCD panel surface (including self-heat)

Note3: Measured at center of LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta = 55°C and RH = 70%

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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	(10.8)	12.0	(13.2)	V	-
Power supply current		IDD	-	TBD Note1	TBD Note2	mA	at VDD = 12.0V, Mode 0 is selected.
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage for Display signals	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-

Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS receiver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

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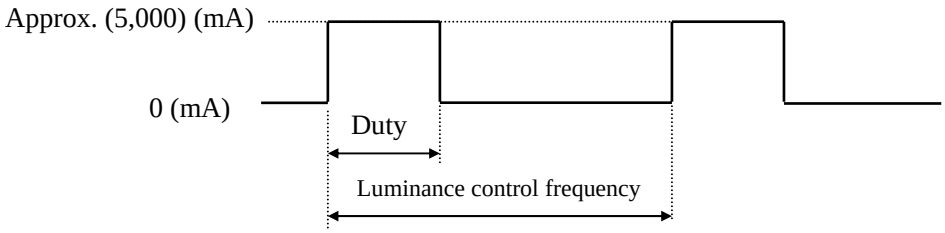
4.3.2 Inverter

(Ta = 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage			VDDB	(11.4)	(12.0)	(12.6)	V	-
Power supply current			IDDB	-	(5,000)	TBD	mA	VDDB = 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	(0.25)	-	(1.0)	V	-
	BRTP signal	High	VBPH	(2.0)	-	(5.25)	V	
		Low	VBPL	(0)	-	(0.8)	V	
	BRTC signal	High	VBCH	(2.0)	-	(5.25)	V	
		Low	VBCL	(0)	-	(0.8)	V	
	PWSEL signal	High	VBSH	(2.0)	-	(5.25)	V	
		Low	VBSL	(0)	-	(0.8)	V	
Input current for signals	BRTI signal		IBI	(-200)	-	(1,000)	μA	
	BRTP signal	High	IBPH	-	-	(1,000)	mA	
		Low	IBPL	(-600)	-	-	mA	
	BRTC signal	High	IBCH	-	-	(400)	μA	
		Low	IBCL	(-600)	-	-	μA	
	PWSEL signal	High	IBSH	-	-	(440)	μA	
		Low	IBSL	(-600)	-	-	μA	

4.3.3 Inverter current wave



At the maximum luminance control: 100%
Minimum luminance control: (20) %
Luminance control frequency: (255) Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of BRTP timing**".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage (See "**4.3.4 Power supply voltage ripple**".) during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

4.3.4 Power supply voltage ripple

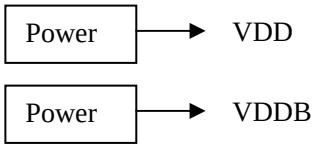
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0 V	≤ 100	mVp-p
VDDB	12.0 V	≤ (200)	mVp-p

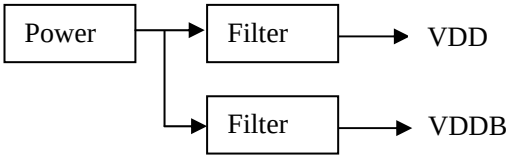
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



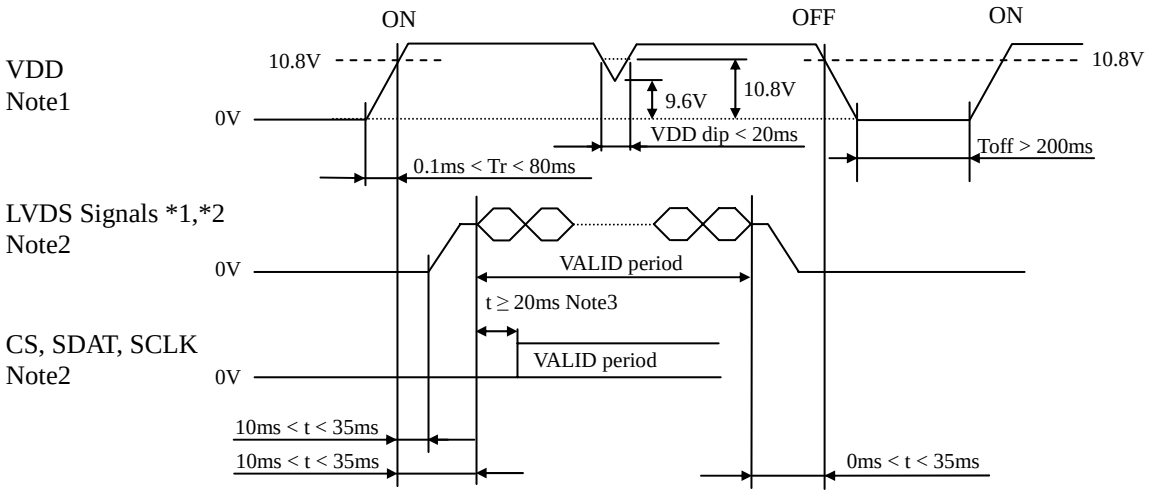
4.3.5 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	TBD	TBD	TBD	TBD	Note1
			TBD		
VDDB	TBD	TBD	TBD	TBD	
			TBD		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE 3

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-,DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

*2: LVDS signals should be measured at the terminal of 100Ω resistance.

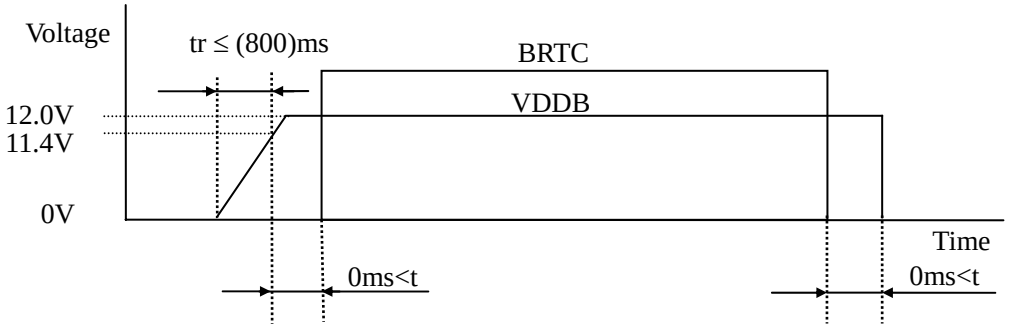
Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: LVDS signals and CS, SDAT, SCLK must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note3: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input.

Note4: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

4.4.2 Inverter



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If tr is more than 800ms, the backlight will be turned off by a protection circuit for inverter.

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

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4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-RE51S (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-RE51HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	Note1
3	GND	Ground	Note1
4	DA0-	Pixel data A0	LVDS differential data input Note2
5	DA0+		
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input Note2
8	DA1+		
9	GND	Ground	Note1
10	DA2+	Pixel data A2	LVDS differential data input Note2
11	DA2-		
12	GND	Ground	Note1
13	CKA+	Pixel clock A	LVDS differential data input Note2
14	CKA-		
15	GND	Ground	Note1
16	DA3+	Pixel data A3	LVDS differential data input Note2
17	DA3-		
18	GND	Ground	Note1
19	DA4-	Pixel data A4	LVDS differential data input Note2
20	DA4+		
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input Note2
23	DB0+		
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input Note2
26	DB1+		
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input Note2
29	DB2+		
30	GND	Ground	Note1
31	CKB-	Pixel clock B	LVDS differential data input Note2
32	CKB+		
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input Note2
35	DB3+		
36	GND	Ground	Note1
37	DB4-	Pixel data B4	LVDS differential data input Note2
38	DB4+		
39	GND	Ground	Note1
40	GND	Ground	Note1

To be continued

Continued 3

Pin No.	Symbol	Signal	Remarks
41	RSEV1	-	Keep this pin Open.
42	RSEV2	-	Keep this pin Open.
43	GND	Ground	Note1
44	RSEV3	-	Keep this pin Open.
45	GND	Ground	Note1
46	RSEV4	-	Keep this pin Open.
47	RSEV5	-	Keep this pin Open.
48	RSEV6	-	Keep this pin Open.
49	RSEV7	-	Keep this pin Open.
50	RSEV8	-	Keep this pin Open.
51	GND	Ground	Note1

Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN2 socket (LCD module side): FI-RE41S (Japan Aviation Electronics Industry Limited (JAE)) 3
Adaptable plug: FI-RE41HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	Note1
3	GND	Ground	Note1
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2+	Pixel data C2	LVDS differential data input Note2
11	DC2-		
12	GND	Ground	Note1
13	CKC+	Pixel clock C	LVDS differential data input Note2
14	CKC-		
15	GND	Ground	Note1
16	DC3+	Pixel data C3	LVDS differential data input Note2
17	DC3-		
18	GND	Ground	Note1
19	DC4-	Pixel data C4	LVDS differential data input Note2
20	DC4+		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CKD-	Pixel clock D	LVDS differential data input Note2
32	CKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	DD4-	Pixel data D4	LVDS differential data input Note2
38	DD4+		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

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CN3 socket (LCD module side): IL-Z-12PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-12S-S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	Note1
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	VDD		
7	GND	Signal ground	Note1
8	GND		
9	GND		
10	GND		
11	GND		
12	GND		

Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 Inverter

CN201 socket (LCD module side): DF3Z-10P-2H (2∗) (HIROSE ELECTRIC Co., Ltd. (HRS))
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co., Ltd. (HRS))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All GNDB and VDDB terminals should be used without any non-connected lines.

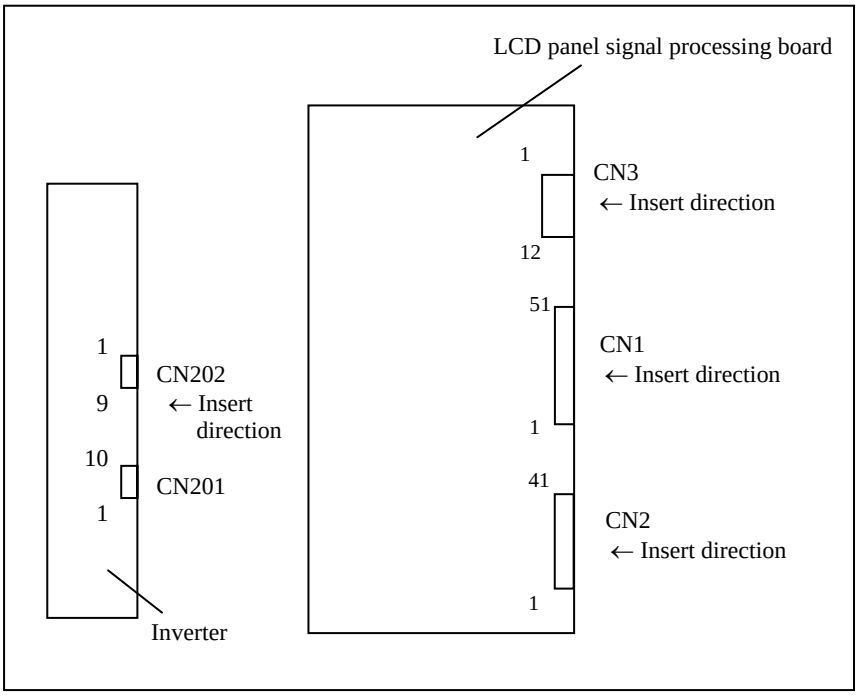
CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	See "**4.6 LUMINANCE CONTROL**".
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	Inverter ground	Note1
9	PWSEL	Selection of luminance control signal method	See "**4.6 LUMINANCE CONTROL** ". Note2

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket 3

Rear side



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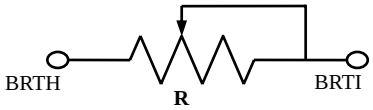
4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL terminal</th><th>BRTP terminal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment
The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.
The resistor (R) must be connected between BRTH-BRTI terminals.
 

• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>1.5 kΩ Note4</td><td>20% (Min. Luminance)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment
Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.
Luminance is the maximum when BRTI terminal is Open.
• Luminance ratio Note3
<table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0.25V Note4</td><td>20% (Min. Luminance)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table></td></tr>
<tr><td>Pulse width modulation

Note1
Note2
Note5</td><td>• Adjustment
Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.
• Luminance ratio Note3
<table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>0.2</td><td>20% (Min. Luminance)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table></td><td>Low</td><td>BRTP signal</td></tr>
</table>

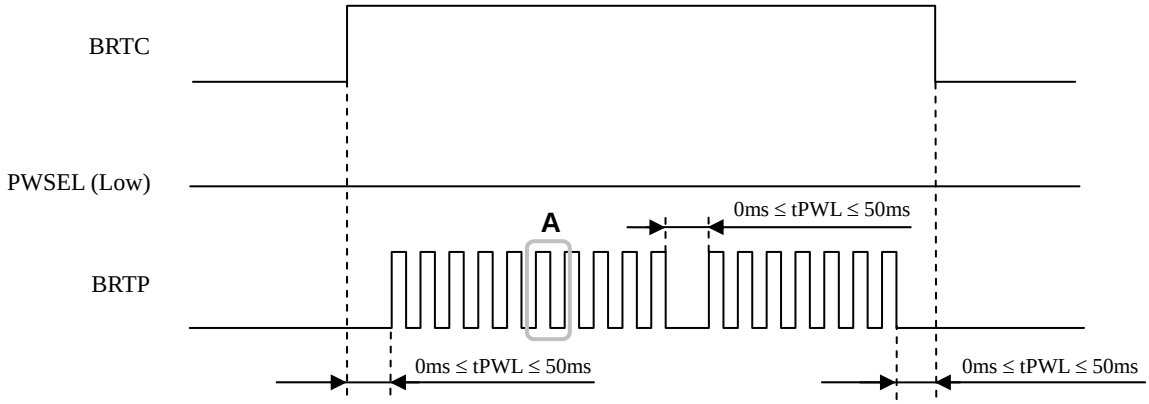
Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.
Use PWM method, if interference noises appear on the display image!
Note2: The inverter will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The inverter will start to work when power is supplied again.
Note3: These data are the target values.
Note4: Do not set the variable resistor and BRTI voltage in less than 1.5kΩ or less than 0.25V. Otherwise flicker or display mura may cause, or the lamp may not be turned on.
Note5: See "**4.6.2 Detail of BRTP timing**".

3

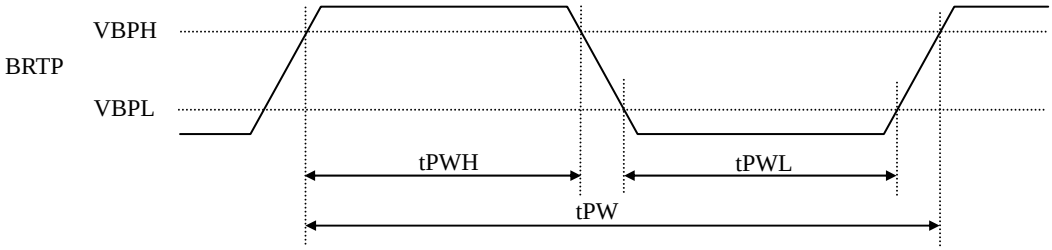
4.6.2 Detail of BRTP timing

(1) Timing diagrams

• Outline chart



• Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	(185)	-	(325)	Hz	Note1, Note2
Duty ratio	DL	(0.2)	-	(1.0)	-	Note1, Note3
Low period	tPWL	0	-	(50)	ms	Note4

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW} \quad DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.
Luminance control frequency = 1/tv × (n+0.25) [or (n + 0.75)]
n = 1, 2, 3 · · · · · ·
tv: Vertical cycle (See "**4.9.1 Timing characteristics**".)

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "**4.6.1 Luminance control methods**".
Note4: If tPWL is more than 50ms, the backlight will be turned off by a protection circuit for inverter. The inverter will start to work when power is supplied again.

3

4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER

	Bit mapping	Transmitter Pin Assignment		Output Connector		CN1	
		Single type LVDS Tx	THine THC63LVD103			Pin No.	Signal name
Pixel data A	LA4	TA0	R14				
	LA5	TA1	R15		Note1		
	LA6	TA2	R16	ATA-	→	4	DA0-
	LA7	TA3	R17	ATA+	→	5	DA0+
	LA8	TA4	R18				
	LA9	TA5	R19				
	CA4	TA6	G14				
	CA5	TB0	G15				
	CA6	TB1	G16				
	CA7	TB2	G17	ATB-	→	7	DA1-
	CA8	TB3	G18	ATB+	→	8	DA1+
	CA9	TB4	G19				
	RA4	TB5	B14				
	RA5	TB6	B15				
	RA6	TC0	B16				
	RA7	TC1	B17				
	RA8	TC2	B18	ATC-	→	10	DA2-
	RA9	TC3	B19	ATC+	→	11	DA2+
	Hsync	TC4	HSYNC				
	Vsync	TC5	VSYNC				
	DE	TC6	DE				
	LA2	TD0	R12				
	LA3	TD1	R13				
	CA2	TD2	G12	ATD-	→	16	DA3-
	CA3	TD3	G13	ATD+	→	17	DA3+
	RA2	TD4	B12				
	RA3	TD5	B13				
	N.C.	TD6	-				
	LA0	TE0	R10				
	LA1	TE1	R11				
	CA0	TE2	G10	ATE-	→	19	DA4-
	CA1	TE3	G11	ATE+	→	20	DA4+
	RA0	TE4	B10				
	RA1	TE5	B11				
	N.C.	TE6	-				
	CLK	CLK	CLK	ATCLK-	→	13	CKA-
				ATCLK+	→	14	CKA+
Pixel data B	LB4	TA0	R14				
	LB5	TA1	R15				
	LB6	TA2	R16	BTA-	→	22	DB0-
	LB7	TA3	R17	BTA+	→	23	DB0+
	LB8	TA4	R18				
	LB9	TA5	R19				
	CB4	TA6	G14				
	CB5	TB0	G15				
	CB6	TB1	G16				
	CB7	TB2	G17	BTB-	→	25	DB1-
	CB8	TB3	G18	BTB+	→	26	DB1+
	CB9	TB4	G19				
	RB4	TB5	B14				
	RB5	TB6	B15				
	RB6	TC0	B16				
	RB7	TC1	B17				
	RB8	TC2	B18	BTC-	→	28	DB2-
	RB9	TC3	B19	BTC+	→	29	DB2+
	Hsync	TC4	HSYNC				
	Vsync	TC5	VSYNC				
	DE	TC6	DE				
	LB2	TD0	R12				
	LB3	TD1	R13				
	CB2	TD2	G12	BTD-	→	34	DB3-
	CB3	TD3	G13	BTD+	→	35	DB3+
	RB2	TD4	B12				
	RB3	TD5	B13				
	N.C.	TD6	-				
	LB0	TE0	R10				
	LB1	TE1	R11				
	CB0	TE2	G10	BTE-	→	37	DB4-
	CB1	TE3	G11	BTE+	→	38	DB4+
	RB0	TE4	B10				
	RB1	TE5	B11				
	N.C.	TE6	-				
	CLK	CLK	CLK	BTCLK-	→	16	CKB-
				BTCLK+	→	15	CKB+

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

	Bit mapping	Transmitter Pin Assignment		Output Connector		CN2	
		Single type LVDS Tx	THine THC63LVD103			Pin No.	Signal name
Pixel data C	LC4	TA0	R14				
	LC5	TA1	R15		Note1		
	LC6	TA2	R16	CTA-	→	4	DC0-
	LC7	TA3	R17	CTA+	→	5	DC0+
	LC8	TA4	R18				
	LC9	TA5	R19				
	CC4	TA6	G14				
	CC5	TB0	G15				
	CC6	TB1	G16				
	CC7	TB2	G17	CTB-	→	7	DC1-
	CC8	TB3	G18	CTB+	→	8	DC1+
	CC9	TB4	G19				
	RC4	TB5	B14				
	RC5	TB6	B14				
	RC6	TC0	B16				
	RC7	TC1	B17				
	RC8	TC2	B18	CTC-	→	10	DC2-
	RC9	TC3	B19	CTC+	→	11	DC2+
	Hsync	TC4	HSYNC				
	Vsync	TC5	VSYNC				
	DE	TC6	DE				
	LC2	TD0	R12				
	LC3	TD1	R13				
	CC2	TD2	G12	CTD-	→	16	DC3-
	CC3	TD3	G13	CTD+	→	17	DC3+
	RC2	TD4	B12				
	RC3	TD5	B13				
	N.C.	TD6	-				
	LC0	TD0	R10				
	LC1	TD1	R11				
	CC0	TD2	G10	CTE-	→	19	DC4-
	CC1	TD3	G11	CTE+	→	20	DC4+
	RC0	TD4	B10				
	RC1	TD5	B11				
	N.C.	TD6	-				
	CLK	CLK	CLK	CTCLK-	→	13	CKC-
				CTCLK+	→	14	CKC+
Pixel data D	LD4	TA0	R14				
	LD5	TA1	R15				
	LD6	TA2	R16	DTA-	→	22	DD0-
	LD7	TA3	R17	DTA+	→	23	DD0+
	LD8	TA4	R18				
	LD9	TA5	R19				
	CD4	TA6	G14				
	CD5	TB0	G15				
	CD6	TB1	G16				
	CD7	TB2	G17	DTB-	→	25	DD1-
	CD8	TB3	G18	DTB+	→	26	DD1+
	CD9	TB4	G19				
	RD2	TB5	B14				
	RD3	TB6	B15				
	RD6	TC0	B16				
	RD7	TC1	B17				
	RD8	TC2	B18	DTC-	→	28	DD2-
	RD9	TC3	B19	DTC+	→	29	DD2+
	Hsync	TC4	HSYNC				
	Vsync	TC5	VSYNC				
	DE	TC6	DE				
	LD2	TD0	R12				
	LD3	TD1	R13				
	CD2	TD2	G12	DTD-	→	34	DD3-
	CD3	TD3	G13	DTD+	→	35	DD3+
	RD2	TD4	B12				
	RD3	TD5	B13				
	N.C.	TD6	-				
	LD0	TE0	R10				
	LD1	TE1	R11				
	CD0	TE2	G10	DTE-	→	37	DD4-
	CD1	TE3	G11	DTE+	→	38	DD4+
	RD0	TE4	B10				
	RD1	TE5	B11				
	N.C.	TE6	-				
	CLK	CLK	CLK	DTCLK-	→	31	CKD-
				DTCLK+	→	32	CKD+

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

4.8 DISPLAY GRAY SCALE AND INPUT DATA SIGNALS

This product can display 1024 gray scales in each LCR sub-pixel and 3072 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display gray scale		Data signal (0: Low level, 1: High level)																															
		LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB9	LB8	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
		LC9	LC8	LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0	CC9	CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	RD9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
		LD9	LD8	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑						:										:										:				
	↓						:										:										:				
	bright	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	↑						:										:										:				
	↓						:										:										:				
	bright	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑						:										:										:				
	↓						:										:										:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

4.9 INPUT SIGNAL TIMINGS

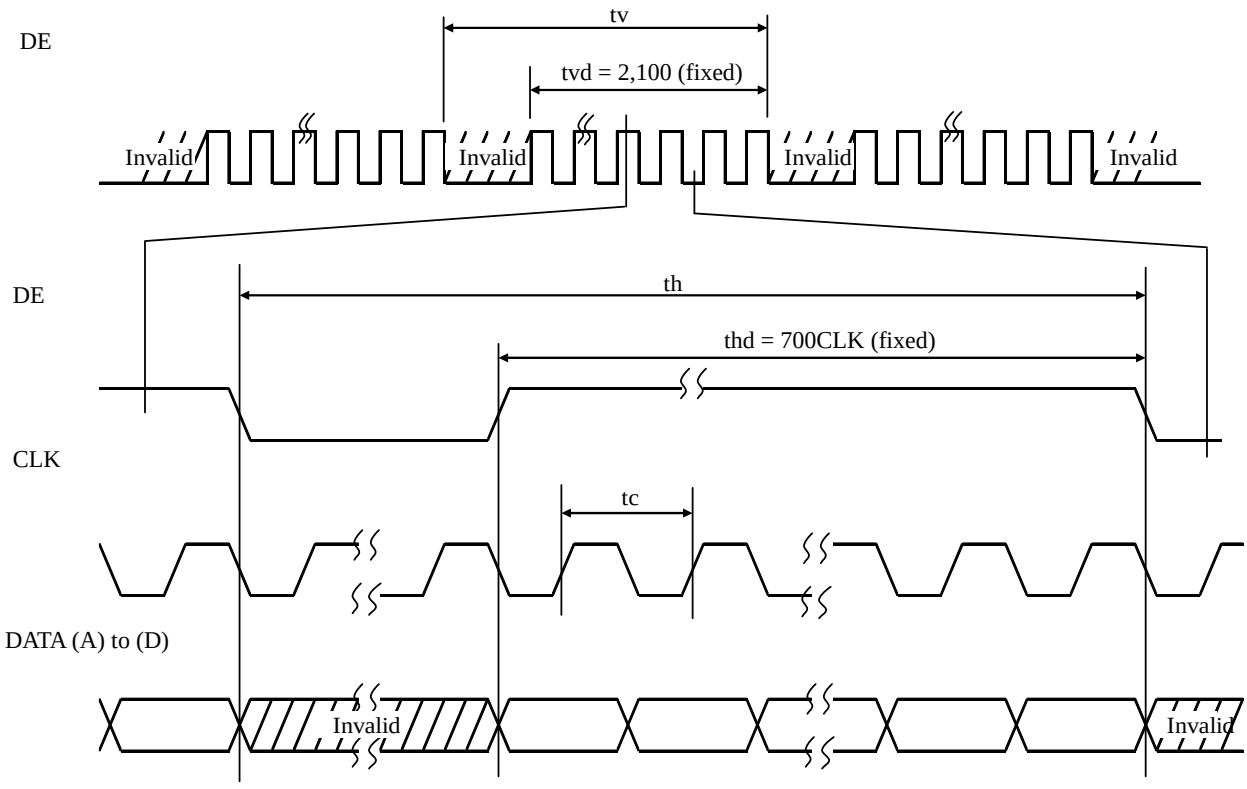
3

4.9.1 Timing characteristics

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	(73)	77.8	TBD	MHz	
	Duty		-	-			-	Note1
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-	-			ns	Note1
		Hold time	-				ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	TBD	9.447	-	µs	105.9 kHz (typ.) Note2
				TBD	735	TBD	CLK	
		Display period	thd	700			CLK	
	Vertical (One frame)	Cycle	tv	-	20.000	TBD	ms	50.0Hz (typ.)
				TBD	2,117	-	H	
		Display period	tvd	2,100			H	
	CLK-DE	Setup time	-	-			ns	Note1
		Hold time	-				ns	
	Rise time, Fall time		-				ns	

Note1: See the data sheet of LVDS transmitter.
Note2: The sum of jitter and skew of horizontal period should be within ±1 CLK.

4.9.2 Input signal timing chart



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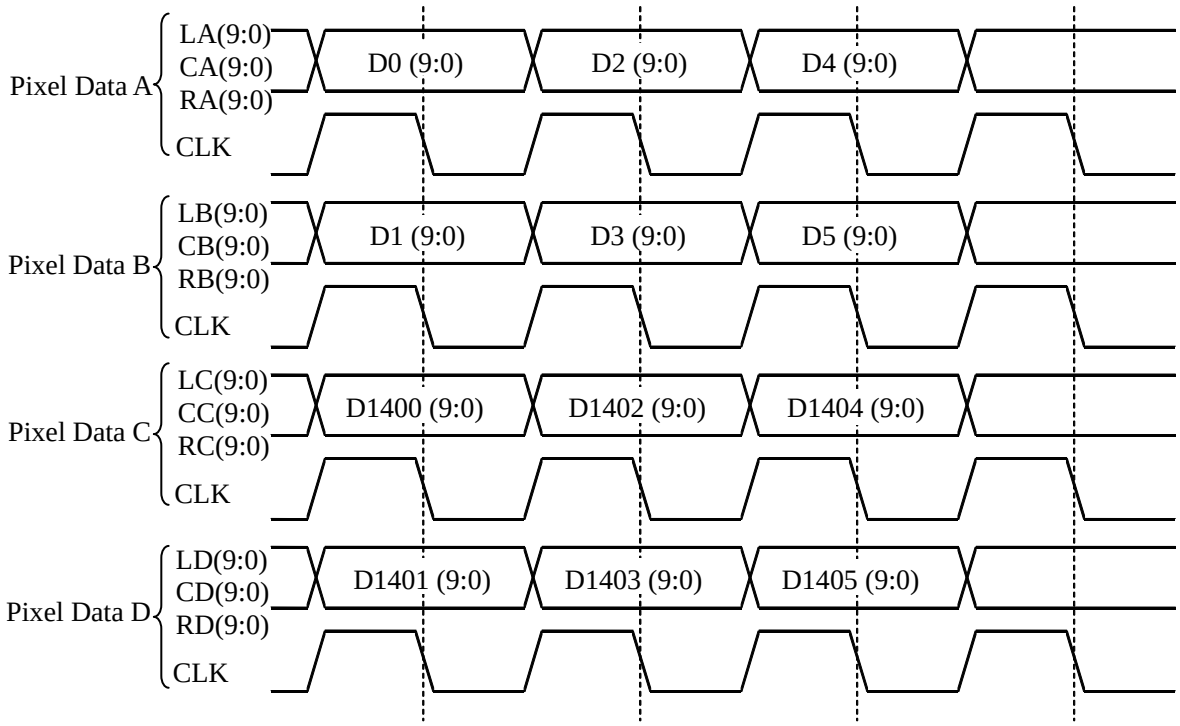
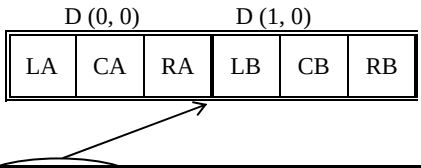
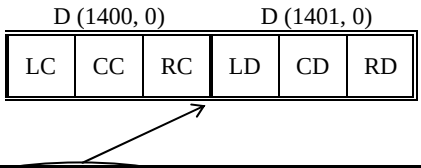
4.10 LVDS DATA TRANSMISSION METHOD



4.11 DISPLAY POSITIONS

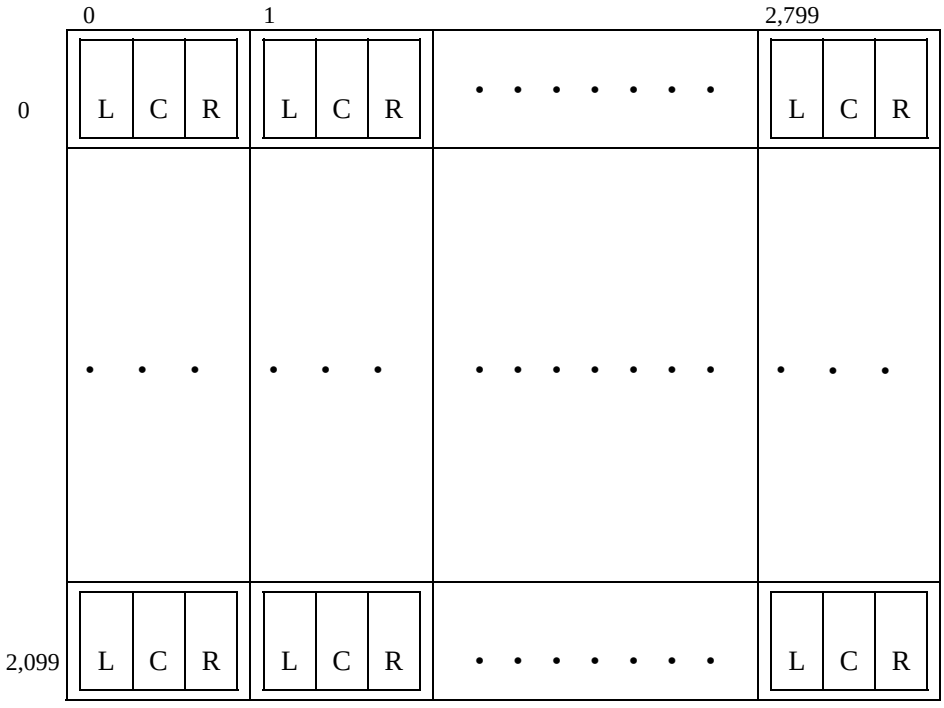
3





0, 0	1, 0	• • •	1398, 0	1399, 0	1400, 0	1401, 0	• • •	2798, 0	2799, 0
0, 1	1, 1	• • •	1398, 1	1399, 1	1400, 1	1401, 1	• • •	2798, 1	2799, 1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0, 2098	1, 2098	• • •	1398, 2098	1399, 2098	1400, 2098	1401, 2098	• • •	2798, 2098	2799, 2098
0, 2099	1, 2099	• • •	1398, 2099	1399, 2099	1400, 2099	1401, 2099	• • •	2798, 2099	2799, 2099

4.12 PIXEL ARRANGNMENT



4.13 OPTICS

4.13.1 Optical characteristics

3

(Note1, Note2)

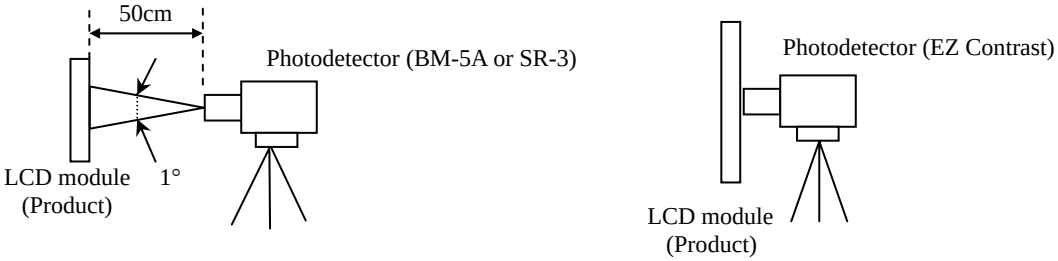
Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	TBD	(1,000)	-	cd/m^2	BM-5A or SR-3	-
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	TBD	(1,000)	-	-	BM-5A or SR-3	Note3
Luminance uniformity		White θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU	-	(1.15)	(1.25)	-	BM-5A or SR-3	Note4
Chromaticity	White	**x** coordinate	Wx	-	0.299	-	-	SR-3	Note5
		y coordinate	Wy	-	0.315	-	-		
Response time		Black to White	Ton	-	TBD	TBD	ms	BM-5A	Note6 Note7
		White to Black	Toff	-	TBD	TBD	ms		
Viewing angle	Right	θU = 0°, θD = 0°, CR ≥ 10	θR	70	85	-	°	EZ Contrast	Note8
	Left	θU = 0°, θD = 0°, CR ≥ 10	θL	70	85	-	°		
	Up	θR = 0°, θL = 0°, CR ≥ 10	θU	70	85	-	°		
	Down	θR = 0°, θL = 0°, CR ≥ 10	θD	70	85	-	°		

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta=25°C, VDD=12V, VDDB=12V, Luminance control = maximum, Display mode: QSXGA+, Horizontal cycle=1/105.9 kHz, Vertical cycle = 1/50.0 Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "**4.13.2 Definition of contrast ratio**".

Note4: See "**4.13.3 Definition of luminance uniformity**".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF=TBD°C

Note7: See "**4.13.4 Definition of response times**".

Note8: See "**4.13.5 Definition of viewing angles**".

4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

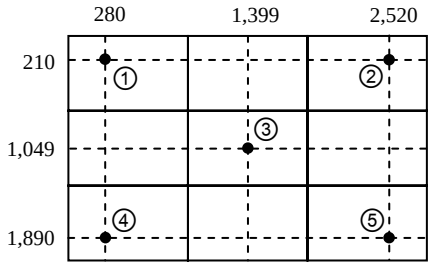
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.13.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

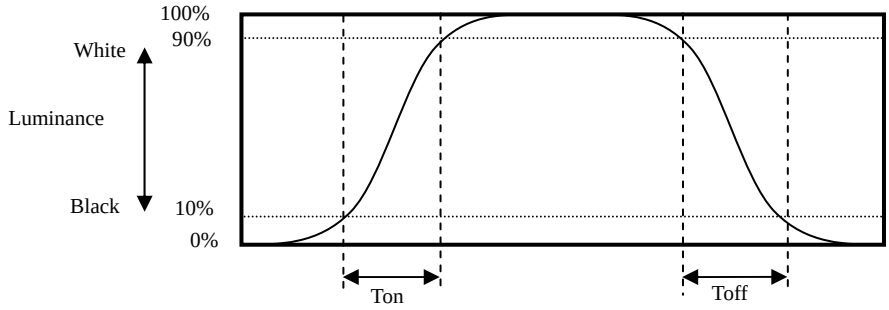
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

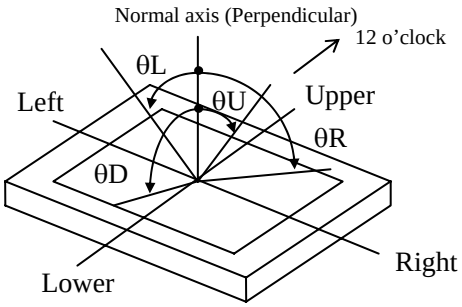


4.13.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.13.5 Definition of viewing angles

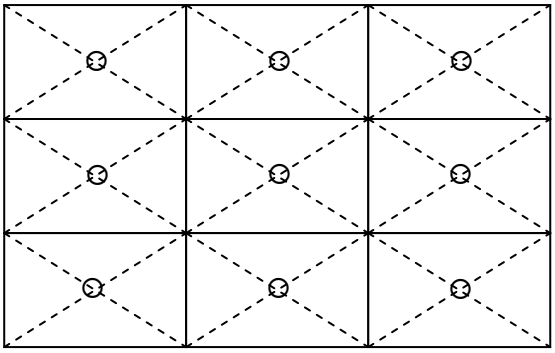


5. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		TBD	No display malfunctions
Heat cycle (Operation)		TBD	
Thermal shock (Non operation)		TBD	
Vibration (Non operation)		TBD	No display malfunctions No physical damages
Mechanical shock (Non operation)		TBD	
ESD (Operation)		TBD	No display malfunctions
Dust (Operation)		TBD	
Low pressure	Non-operation	TBD	No display malfunctions
	Operation	TBD	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

- **Do not touch the working backlight. There is a danger of an electric shock.**

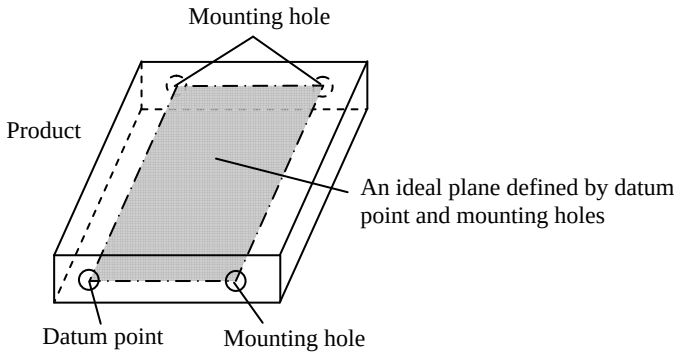
- **Do not touch the working backlight. There is a danger of burn injury.**
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater TBDm/s^2 and to be not greater TBDms, Pressure: To be not greater 19.6N (ϕ16mm jig))**

6.3 ATTENTIONS 

6.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed TBDN·m. Higher torque might result in distortion of the bezel.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura. Recommended installing method: An ideal plane that is defined by datum point and mounting holes is to be the same plane within ±0.3 mm.



⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
⑧ Do not push nor pull the interface connectors while the product is working.
⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.

6.3.3 Characteristics

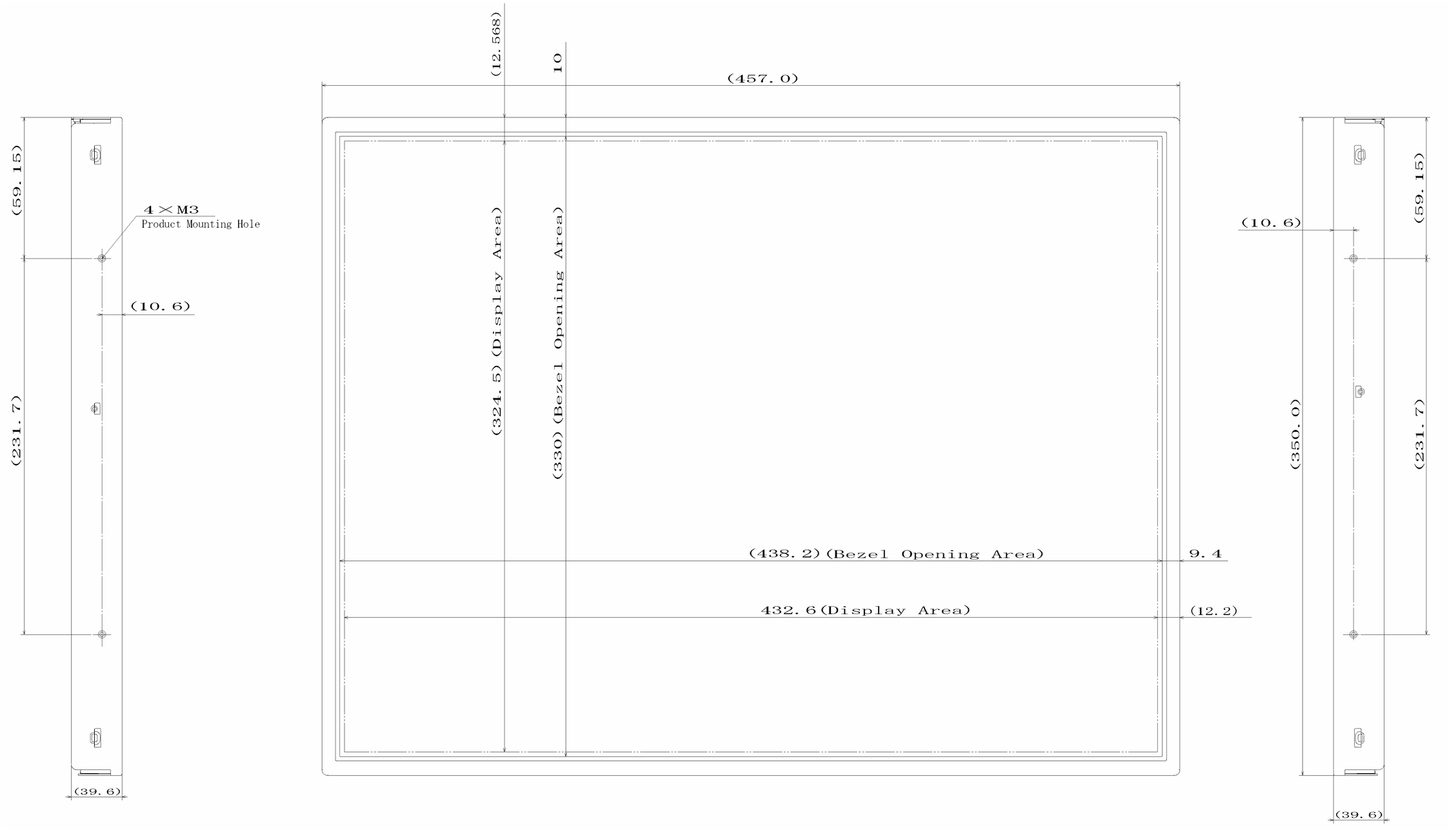
The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed depending on input signal timings.
⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

6.3.4 Other

① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ See "REPLACEMENT MANUAL FOR BACKLIGHT UNIT", when replacing backlight lamps.
④ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

7. OUTLINE DRAWINGS



Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-MD-0066	May 17, 2006	**Revision contents** New issue **Writer** *Approved by* T. OGAWA *Checked by* ——— *Prepared by* T. OGAWA
2nd edition	DOD-MD-0073	May 22, 2006	**Revision contents** P5 General specifications • Weight: → (3,500)g (typ.) • Contrast ratio: → (1,000:1) (typ.) • Polarizer surface: → Antiglare • Polarizer pencil-hardness: → 4H (min.) [by JIS K5400] • Power consumption: → (71)W (typ.) P6 Block diagram: VDDB, BRTC, BRTH, BRTI, BRTP, PWSEL, GNDB (addition) P7 • Mechanical specifications- Weight: → (3,500)g (typ.) • Absolute maximum ratings • Storage temperature (Tst): → -20 to +60°C • Operating temperature- Front surface (TopF): → 0 to +55°C - Rear surface (TopR): → 0 to +60°C • Operating altitude, Storage altitude (addition) P26 Optical characteristics • Contrast ratio (CR): → (1,000) (typ.) • Luminance uniformity: → (1.15) (min.), (1.25) (typ.) • Luminance uniformity- Measuring instrument: SR-3 (addition) P27 Definition of luminance uniformity: diagram (correction) P32 Outline drawings (addition) **Writer** *Approved by* T. OGAWA *Checked by* ——— *Prepared by* T. OGAWA
3rd edition	DOD-PP-0006	July 12, 2006	**Revision contents** Data correction or implementation depend on the specification review P1 Type name is decided. NL280210AM15-01 P4 Features P5 General specifications P6 Block diagram P7 Detailed specifications P8-P9 Electrical characteristics P11 Power supply voltage sequence P12-P16 Connections and functions for interface pins P17-P18 Luminance control P19-P20 Method of connection for LVDS transmitter P22 Input signal timings P23 LVDS data transmission method P24 Display positions P25 Optical characteristics P31 Outline drawings

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-0006	July 12, 2006	**Revision contents** **Signature of writer** *Approved by* T. OGAWA *Checked by* *Prepared by* N. KANO