HITACHI

Hitachi Displays, Ltd.

DATE: Mar. 28, 2003

TECHNICAL DATA

TENTATIVE SPECIFICATIONS OF
7" WIDE-VGA TFT-LCD MODULE

TX18D16VM1CAA

CONTENTS

Notes :

1. The information contained herein is tentative and may be changed without prior notices.
2. Please contact Hitachi before proceeding to the design of your product.

RECORD OF REVISION

Date	Sheet No.	Summary
Mar.28, 2003	3284LTD-1502-2 Page 4-1/1	1.1 ENVIRONMENTAL ABSOLUTE MAXIMUM RATIONGS Temperature Operation : Min. -20℃ → 0℃, Max. 75℃ → 70℃ Non-operation : Min. -30℃ → -20℃, Max. 85℃ → 70℃
		1.2 (2)BACK-LIGHT UNIT Lamp Current Max.6.5mArms → 7.0mArms
	3284LTD-1502-2 Page 5-1/2	2.OPTICAL CHARACTERISTICS Revision of Color Position on CIE

DESCRIPTION

The specifications are applied to the following TFT Liquid Crystal Display Module with Back-light unit.

Note : Inverter device for Back-Light is not built in so it should be prepared by yourself.

General Specifications

Type Name	TX18D16VM1CAA	
Effective Display Area	H 152.4 x V 91.44	[mm]
Display Dots	H(800x3) x V 480	[dots]
(Display Pixels)	(H 800 x V 480)	[pixels]
Pixel Pitch	H 0.1905 x V 0.1905	[mm]
Color Pixel Arrangement	R·G·B Vertical Stripe	
Display Mode	Transmissive Mode, Normally White Mode	
Surface Polarizing Film	Polarizing Film with Antiglare Coating	
Number of Colors	262k	[colors]
Interface	C-MOS, R.G.B x 6 bit Digital each	
Color Saturation	60%(typ.) for NTSC	
Viewing Angle	12:00 Direction	
Backlight	CFL, 1pc Side-light type	
Dimensions Outline	H 165.0(typ.) x V 106.0(typ.) x t10.5(max.)	[mm]
Weight	Approximately 170	[g]

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operation		Non-operation		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	70	-20	70	℃	1)
Humidity	2)		2)		%RH	1)
Vibration	—	4.9 (0.5G)	—	19.6 (2G)	m/s2	3)
Shock	—	29.4 (3G)	—	490 (50G)	m/s2	4)
Corrosive Gas	Not Acceptable		Not Acceptable			
Illumination at LCD Surface	—	50,000	—	50,000	lx	

Notes 1) "Temperature" and "Humidity" shall be at glass surface of a TFT-LCD Module, not in the system installed with the Module.
At low temperature the brightness of CFL drop and the life time of CFL become to be short.
Operating temperature range at -40~85℃:No damege for short time is T.B.D.
2) Ambient temp. Ta≦40 ℃ : 85 % RH Max. Without condensation.
Ta>40 ℃ : Absolute humidity must be lower than the humidity of 85 % RH at 40 ℃. without condensation.
3) Frequency of the vibration shall be between 20 Hz and 50 Hz. (except resonance point)
4) Pulse width of the shock shall be 7 ms.

1.2 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

VSS=0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage for logic	VDD	0	4.3	V	
Input signal Voltage for logic	VI	-0.2	VDD+0.2	V	1)
Electrostatic Durability	VESD0	±100		V	2), 3)
	VESD1	±8		kV	2), 4)

Notes 1) The specification shall be applied to pixel data signal and clock signal.
2) Discharge circuit to be connected : 200 pF - 250 Ω, Environmental : 25℃ - 70 % RH
3) The specification shall be applied to I/F connector pins.
4) The specification shall be applied to the surface of both a metal bezel and a LCD panel.

(2) BACK-LIGHT UNIT

GND=0V

Item	Symbol	Min.	Max.	Unit	Note
Lamp Current	IL	-	7.0	mArms	1)
Lamp Voltage	VL	-	2000	Vrms	2)

Notes 1) To be measured at GND terminal side
2) The specification shall be applied at connector pins for back-light units at start-up.

2. OPTICAL CHARACTERISTICS

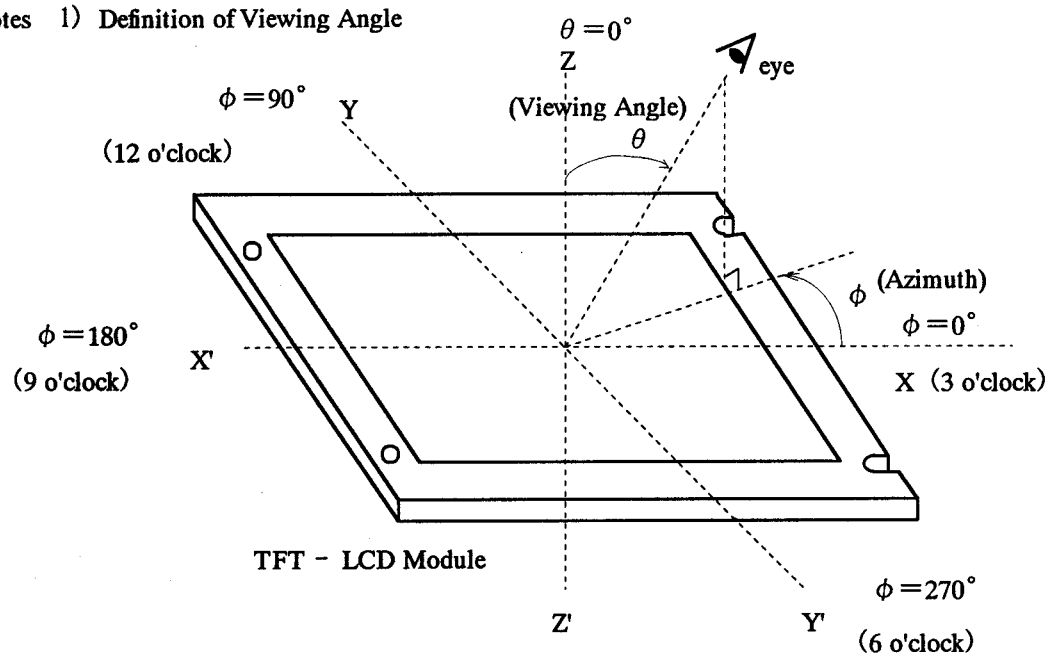
The following optical characteristics shall be measured during operation of the unit (TFT-LCD module and Back-Light) on the condition the measuring systems operation are stable. It takes about 15 minutes. The measured point shall be at the center of the LCD unless any specified. The ambient light excluding light from the backlight unit of the module shall be prohibited.

- Measuring equipment : Pritchard 1980A, or equivalent

Temperature of LCD = 25 ℃, VDD = 3.3 V, fV = 60 Hz, IL= 4.0mA

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		100	200	—		2)
Response Time	RISE	tr		—	20	30	ms	3)
	FALL	tf		—	10	20	ms	3)
Brightness (White)		Bwh		300	350	—	cd/m2	
Brightness Uniformity		Buni		70	—	—	%	4)
Color Position on CIE	Red	x	θ =0℃ 1)	0.58	0.63	0.68	—	
		y		0.29	0.34	0.39		
	Green	x		0.24	0.29	0.34		
		y		0.54	0.59	0.64		
	Blue	x		0.09	0.14	0.19		
		y		0.03	0.08	0.13		
	White	x		0.25	0.30	0.35		
		y		0.27	0.32	0.37		
Viewing Angle (CR≧10)	x − x'	θ x	θ =0°	50	—	—	deg.	1)
		θ x'	θ =180°	50	—	—		
	y − y'	θ y	θ =90°	50	—	—		
		θ y'	θ =270°	50	—	—		

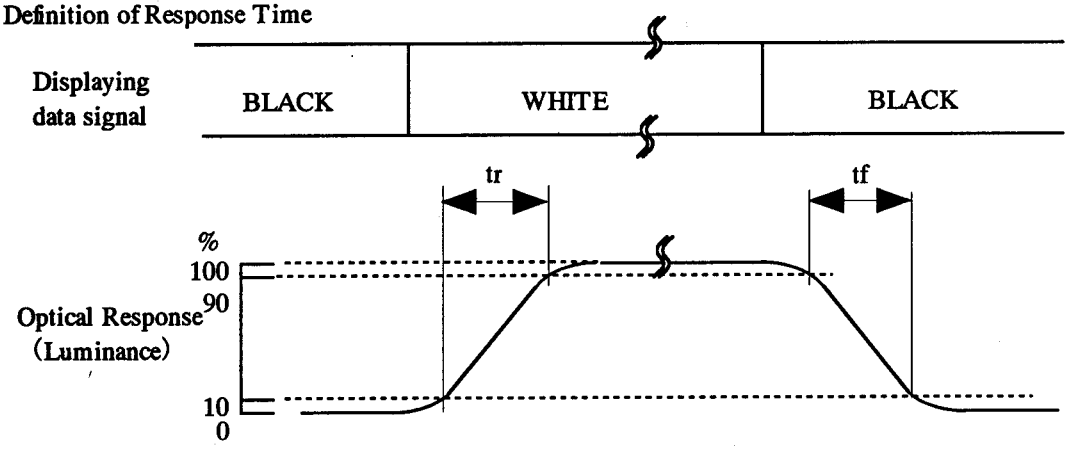
Notes 1) Definition of Viewing Angle



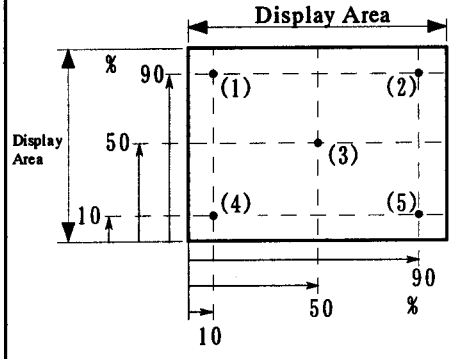
2) Definition of Contrast Ratio(CR):

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



• :measuring point

The brightness uniformity (Buni) is defined as the following equation.

$$Buni = \frac{Bmin}{Bmax} \times 100$$

where, Bmax = Maximum brightness among 5 measuring points
Bmin = Minimum brightness among 5 measuring points

3. ELECTRICAL CHARACTERISTICS

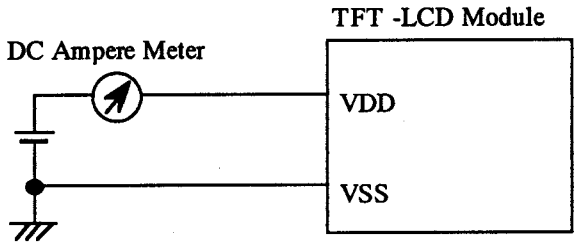
3.1 TFT LIQUIDO CRYSTAL DISPLAY MODULELE

Ta=25℃, VSS=0V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage		VDD	3.0	3.3	3.6	V	
Input Voltage for Logic Circuits	Hi	VIH	2.0	—	VDD	V	1)
	Lo	VIL	VSS	—	0.8	V	1)
Power Supply Current		IDD	—	250	350	mA	2), 3)
VSYNC Frequency		fV	—	60	75	Hz	
HSYNC Frequency		fH	—	31.6	39.2	kHz	
DCLK Frequency		fCLK	—	33.3	40	MHz	

Notes 1) Display data pins and Timing signal pins are subjected.

2) fV=60Hz, fCLK=33.3 MHz, VDD=3.3V, DC Current.



Typical value is measured when displaying Black raster.

Maximum is measured when displaying Vertical-stripe pattern.

3) Current capacity for VDD power source should be larger than (1)A.

3.2 BACK-LIGHT UNIT

Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Lamp Current	IL	2.0	3.0	4.0	mArms	1),3)
Lamp Voltage	VL	—	1000	—	Vrms	
Frequency	fL	50	—	70	kHz	2)
Starting Lamp Voltage	VS	1400	—	—	Vrms	Ta=25deg. C
		1700	—	—		Ta=-20deg. C

Notes

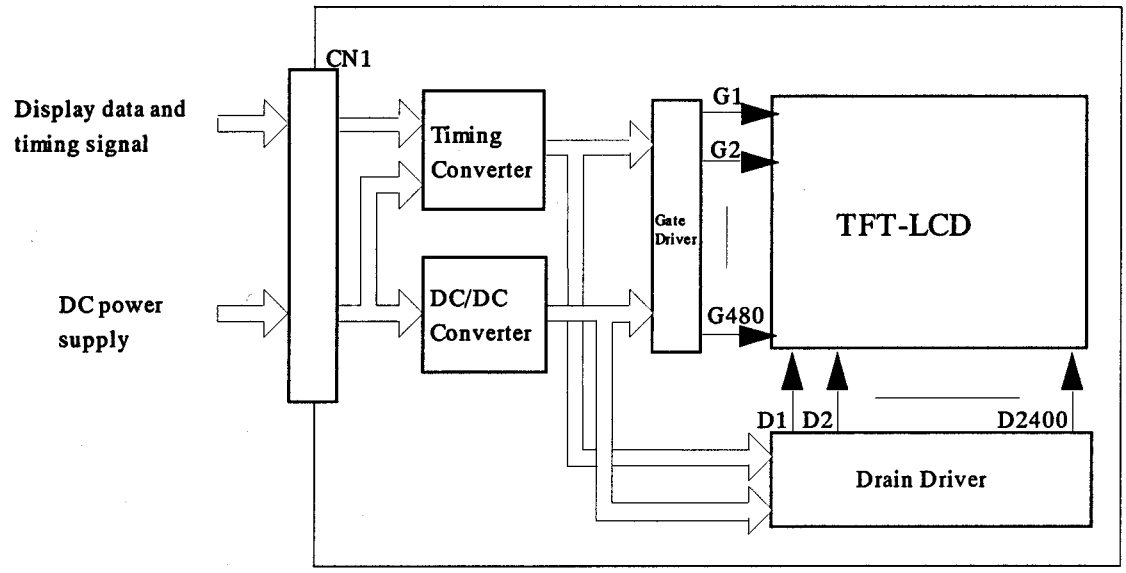
1) Larger IL causes the shorter life of a lamp CFL.

2) Frequency of power supply for a CFL may cause interference with HSYNC frequency and causes beat or flicker on the display. Therefore, lamp frequency shall be as different as possible from HSYNC frequency in order to avoid the interference.

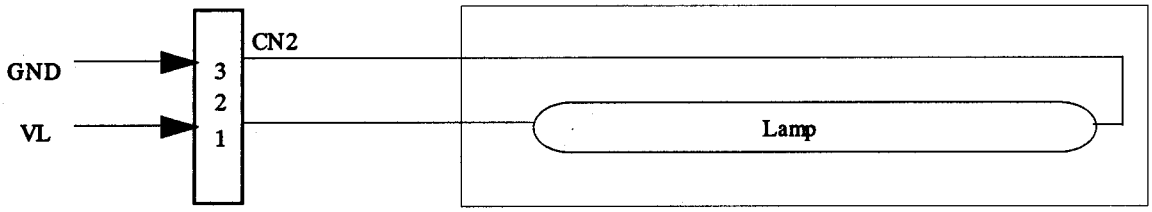
3) To be measured at GND terminal side

4. BLOCK DIAGRAM

4.1 TFT-LCD MODULE



4.2 BACK-LIGHT UNIT



Color of wires from CFL to CN2

3 (GND) : White
1 (VL) : Pink

5. INTERFACE PIN CONNECTION

5.1 TFT-LCD MODULE

CN1 《JAE ; FA5B040HF1R3000》

Pin No.	Symbol	Description	Note
1	VDD	Power Supply (typ.+3.3V)	1)
2	VDD		
3	VDD		
4	VDD		
5	(NC)	Non-Connect	4)
6	DTMG	Display Timing	
7	VSS	GND (0V)	2)
8	(NC)	Non-Connect	4)
9	VSS	GND (0V)	2)
10	(IC)		3)
11	VSS	GND (0V)	2)
12	B5	Blue Data	
13	B4		
14	B3		
15	VSS	GND (0V)	2)
16	B2	Blue Data	
17	B1		
18	B0		
19	VSS	GND (0V)	2)
20	G5	Green Data	
21	G4		
22	G3		
23	VSS	GND (0V)	2)
24	G2	Green Data	
25	G1		
26	G0		
27	VSS	GND (0V)	2)
28	R5	Red Data	
29	R4		
30	R3		
31	VSS	GND (0V)	2)
32	R2	Red Data	
33	R1		
34	R0		
35	(IC)		3)
36	VSS	GND (0V)	2)
37	VSS		
38	DCLK	Dot Clock	
39	VSS	GND (0V)	2)
40	VSS		

Notes 1) All VDD pins shall be connected to +3.3V(Typ.).
2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.
3) Keep open. Hitachi test use only.
4) Unconnected to the module

5.2 BACK-LIGHT UNIT

CN2 《J.S.T. ; BHR-03VS-1》

Pin No.	Symbol	Description	Note
1	VL	Power Supply	
2	NC	No connection	
3	GND	GND(0V)	

5.3 RELATIONSHIP BETWEEN DISPLAYED COLOR AND INPUT DATA

Color	Input	Red Data						Green Data						Blue Data					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenda	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (2)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green (2)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Notes 1) Definition of gray scale:

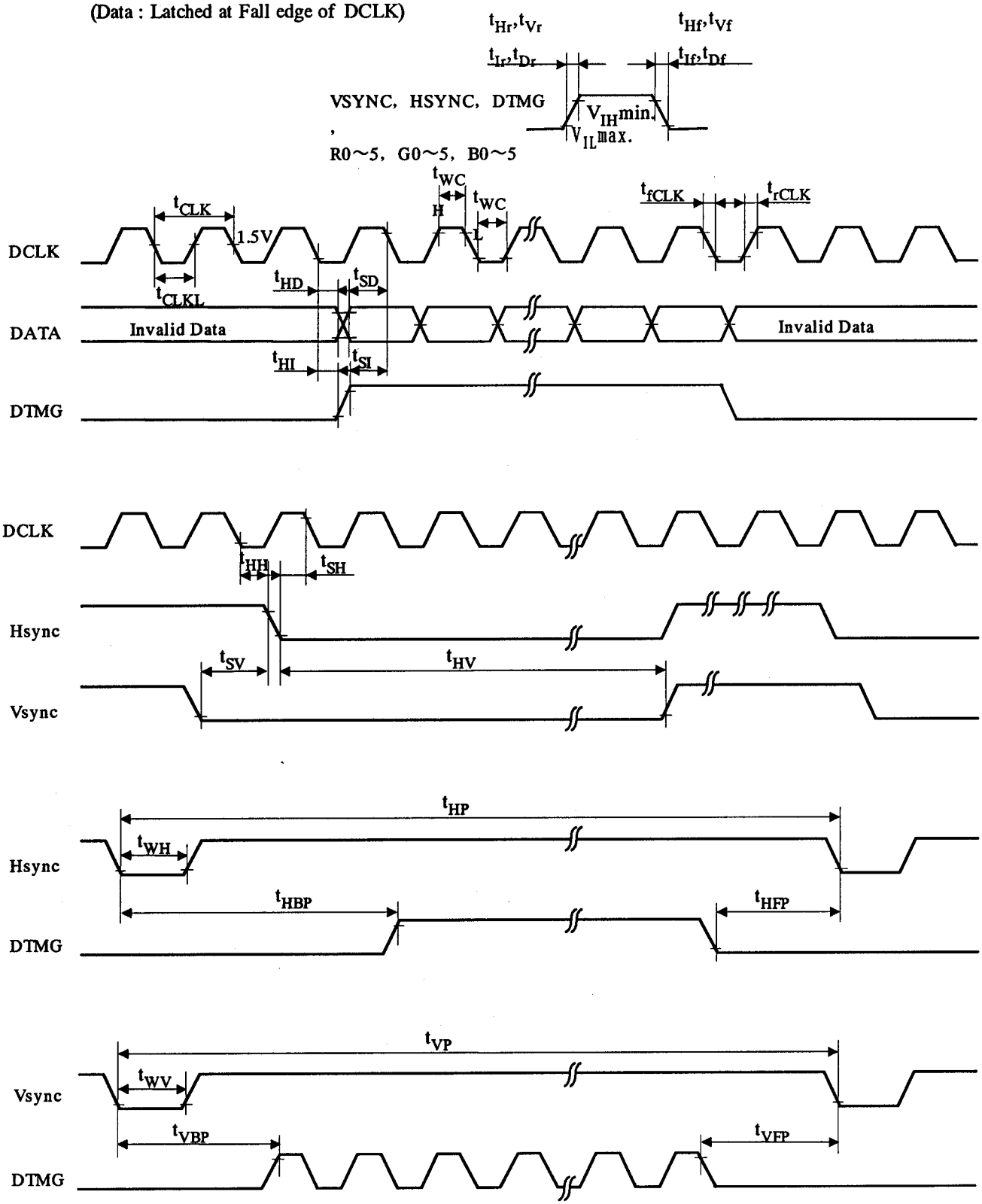
Color(n) • • • • Number in parenthesis indicates gray scale level. Lower n corresponds to brighter level.

2) Data: 1:High, 0:Low

6. INTERFACE TIMING

6.1 TIMING CHART

(Data : Latched at Fall edge of DCLK)

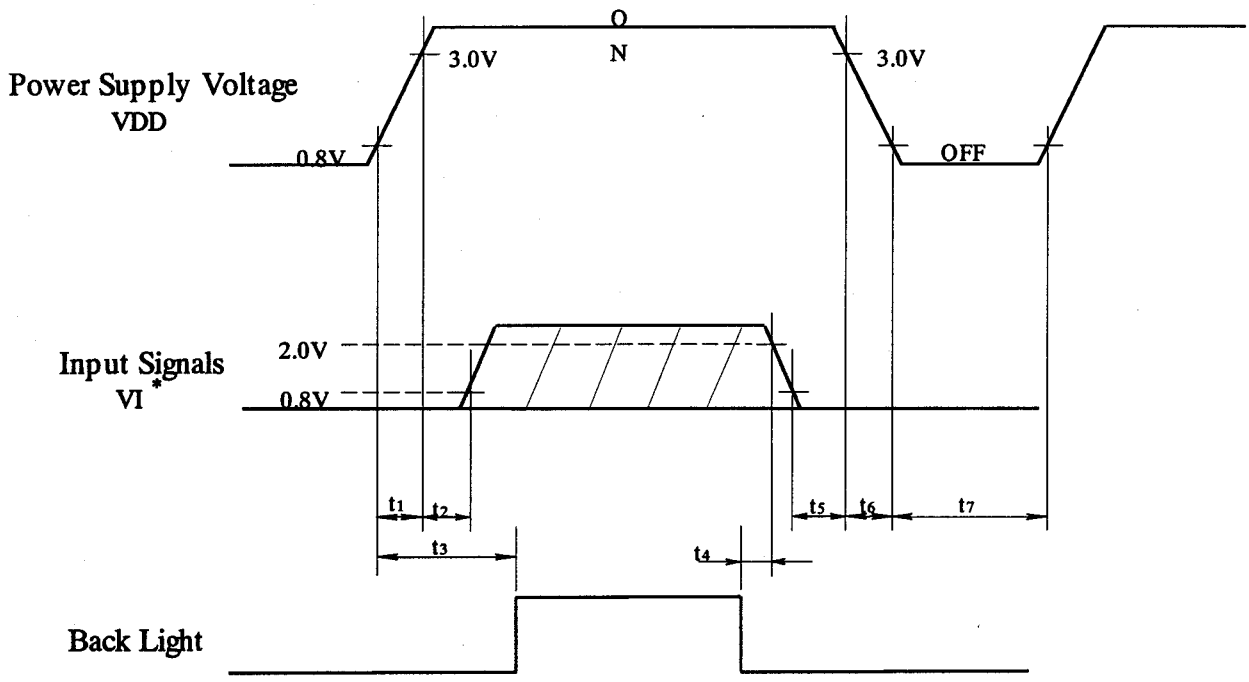


* The DTMG signal for this module is defined as above-mentioned timings for Vsync and Hsync.
This module synchronizes with only DTMG and don't require inputting Vsync and Hsync signals.
During Blanking priod, DTMG should be "Low" level

6.2 INTERFACE TIMING SPECIFICATIONS

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Period	t_{CLK}	25	30	33	ns	
	Width-Low	t_{WC}	12	—	—		
	Width-Hi	t_{WCH}	12	—	—		
	Rise Time	t_{rCLK}	—	—	25		
	Fall Time	t_{fCLK}	—	—	25		
	Duty	D	0.45	0.5	0.55	—	$D=t_{CLKL}/t_{CLK}$
Hsync	Set up Time	t_{SH}	5	—	—	ns	for DCLK
	Hold Time	t_{HH}	10	—	—		
	Period	t_{HP}	944	1056	1088	t_{CLK}	
	Width-Active	t_{WH}	4	128	—		
	Rise/Fall Time	t_{Hr},t_{Hf}	—	—	30	ns	
Vsync	Set up Time	t_{SV}	0	—	—	t_{CLK}	for Hsync
	Hold Time	t_{HV}	2	—	—		
	Period	t_{VP}	515	525	610	t_{HP}	
	Width-Active	t_{WV}	1	2	—		
	Rise/Fall Time	t_{Vr},t_{Vf}	—	—	50	ns	
DTMG	Set up Time	t_{SI}	5	—	—	ns	for DCLK
	Hold Time	t_{HI}	10	—	—		
	Rise/Fall Time	t_{Ir},t_{If}	—	—	30	ns	
	Horizontal Back porch	t_{HBP}	7	88	—	t_{CLK}	
	Horizontal Front porch	t_{HFP}	—	40	—		
	Vertical Back porch	t_{VBP}	4	32	—	t_{HP}	
	Vertical Front porch	t_{VFP}	—	11	—		
DATA	Set up Time	t_{SD}	5	—	—	ns	for DCLK
	Hold Time	t_{HD}	10	—	—		
	Rise/Fall Time	t_{Dr},t_{Df}	—	—	25	ns	

6.3 TIMING BETWEEN INTERFACE SIGNAL AND POWER SUPPLY



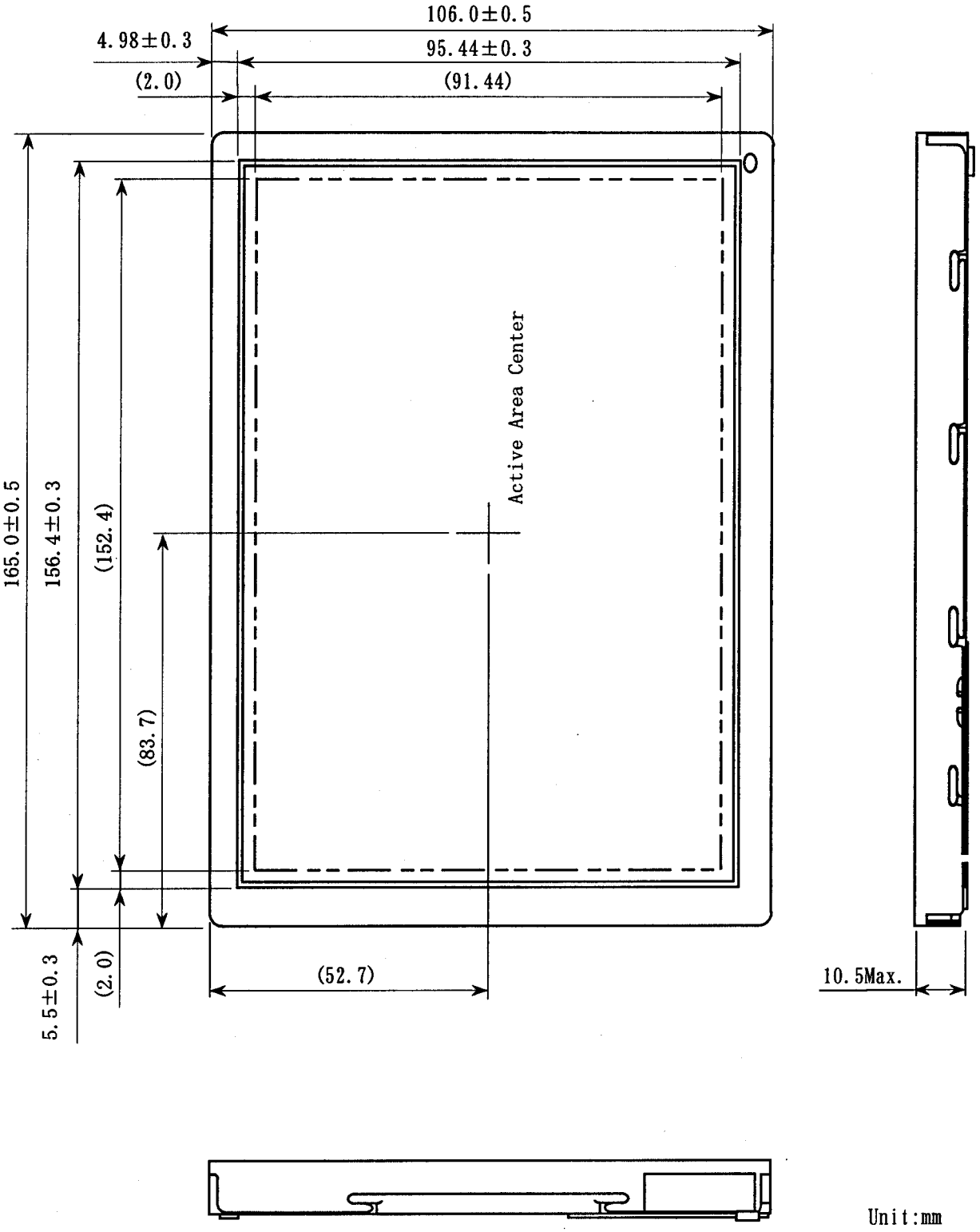
POWER ON	POWER OFF
$t_1 \leqq 15ms$	$5ms \leqq t_4$
$0ms < t_2 \leqq 45ms$	$0ms \leqq t_5 \leqq 45ms$
$0.1s \leqq t_3$	$0ms \leqq t_6 \leqq 20ms$
	$0.4s \leqq t_7$

* Set $0V \leqq VI(t) \leqq VDD(t)$.
Here, VI(t), VDD(t) indicate the transitive state of VI, VDD when power supply is turned ON or OFF.

Note 1) Do not keep interface signal high-impedance when power on.

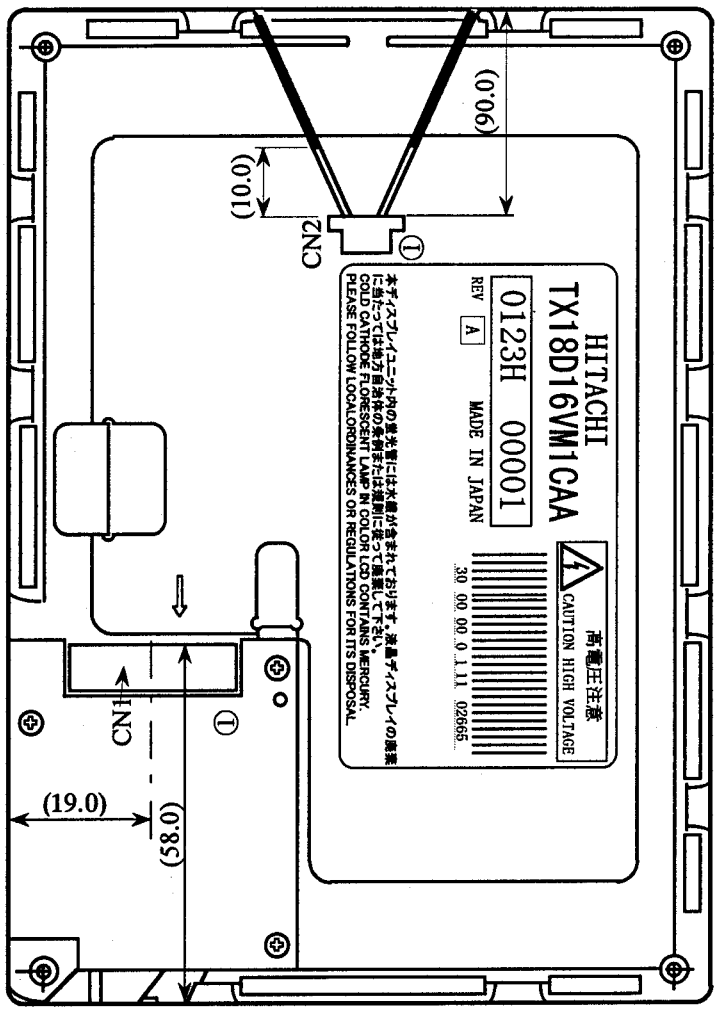
7. Dimentional Outline

7.1. Surface side



Unit:mm

7.2. Back side



Note1)CN1:FA5B040HF1R3000(JAE)

2)CN2:BHR-03VS-1(JST)

Unit:mm

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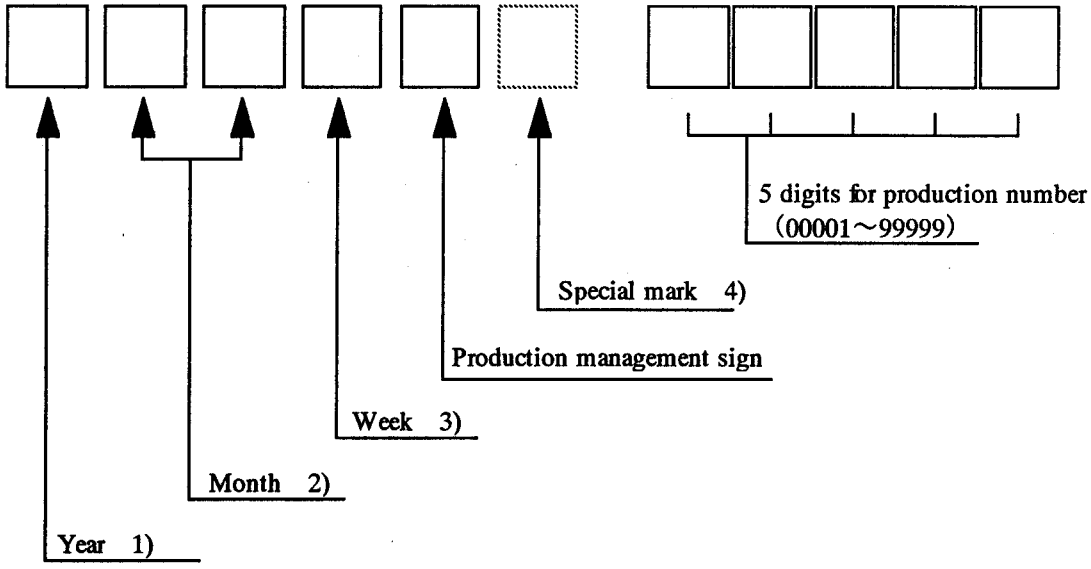
8. DESIGNATION OF LOT MARK

8.1 LOT MARK



Notes

1)

Year	Mark
2003	3
2004	4
2005	5
2006	6
2007	7

2)

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

3)

Week (Days)	Mark
1～7	1
8～14	2
15～21	3
22～28	4
29～31	5

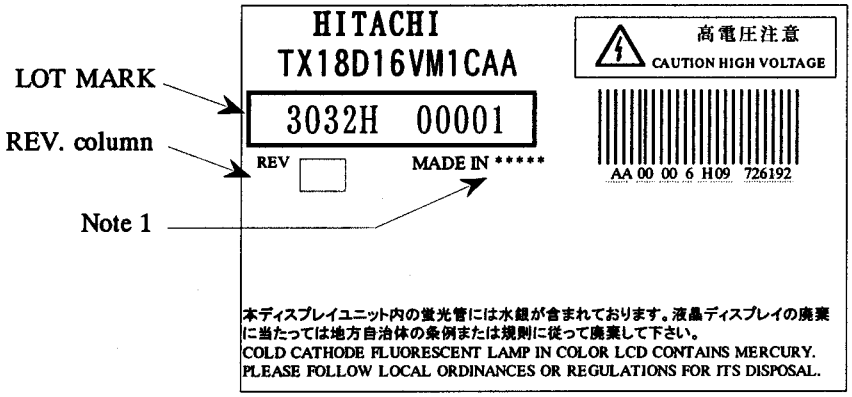
4) The special mark may be added by manufacturing accordingly to production number.

8.2 REVISION(REV.) CONTROL

REV. column is controlled by the manufacturing. A-Z except I and O is to be written on this column.

8.3 LOCATION OF LOT MARK

Lot mark is printed on a label.The label is on rear side of module as shown in the drawing at Section 7.
The style of character may be changed without notice.



Note 1 Product Country

Product Country	Print on Label
JAPAN	JAPAN
TAIWAN	TAIWAN R.O.C.

Product Country on the Label shall be printed as shown in above Fig. based on product country.

8. 4 Example of product label

8.4.1 Made in JAPAN

8.4.2 Made in TAIWAN R.O.C